



P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Third Semester, B.E. - Electronics and Communication Engineering
Semester End Examination; Dec - 2017/Jan - 2018

Digital Electronic Circuits

Time: 3 hrs

Max. Marks: 100

Note: Answer FIVE full questions, selecting ONE full question from each unit.

UNIT - I

- | | | | |
|---|----|---|----|
| 1 | a. | Explain gate performance properties with relevant equations and diagrams. | 8 |
| | b. | Explain with circuit diagram the operation of two input TTL NAND gate. | 7 |
| | c. | What is the significance of wired logic in TTL explain with suitable diagram. | 5 |
| 2 | a. | Construct a two input CMOS NAND gate and explain its working principle. | 10 |
| | b. | Explain the operation of an NMOS inverter with neat diagrams. | 10 |

UNIT - II

- | | | | |
|---|----|---|----|
| 3 | a. | Find the minimal sum expression for the following incomplete Boolean functions using k-map: $f(w, x, y, z) = \Pi M(2, 8, 11, 15) + dc(3, 12, 14)$. | 7 |
| | b. | Transform each of the following canonical expressions into its other canonical form in decimal notations: | 5 |
| | | i) $f(x, y, z) = \Pi M(3, 4)$ ii) $f(w, x, y, z) = \sum m(0, 1, 2, 3, 7, 9, 11, 12, 15)$. | |
| | c. | Identify all the prime implicants and essential prime implicants of the following function using K-map: | 8 |
| | | i) $f(a, b, c, d) = \bar{a}\bar{c}d + \bar{a}cd + \bar{b}\bar{c}\bar{d} + a\bar{b}c + \bar{a}\bar{b}c\bar{d}$ | 8 |
| | | ii) $f(a, b, c, d) = (a + b + \bar{d})(\bar{a} + b + \bar{d})(a + \bar{b} + \bar{c} + d)(\bar{a} + \bar{b} + \bar{c} + \bar{d})(\bar{a} + \bar{b} + \bar{c} + d)$ | |
| 4 | a. | Find all the prime implicants of the function using Quine-McClusky algorithm; | 10 |
| | | $f(a, b, c, d) = \Pi m(0, 2, 3, 4, 5, 12, 13) + dc(8, 10)$ | |
| | b. | For the given Boolean function apply MEV technique to obtain minimal sum and minimal product expressions. | 10 |
| | | $f = \sum m(3, 4, 5, 7, 8, 11, 12, 13, 15)$. | |

UNIT - III

- | | | | |
|---|----|---|---|
| 5 | a. | Describe the principle of operation of a 4-bit binary adder / subtractor with a block diagram. | 7 |
| | b. | Realize the following Boolean expression using an active high decoder. The gate should be selected to minimize the total number of input terminals. | 5 |
| | | $f_1(x_2, x_1, x_0) = \sum m(0, 1, 3, 4, 5, 6)$ $f_2(x_2, x_1, x_0) = \sum m(1, 2, 3, 4, 6)$ | 5 |

- c. Describe the principle of 8-to-3 line encoder. Why priority encoders are developed? With the condensed truth table for 8-to-3 line priority encoder. 8
- 6 a. Realize the Boolean expression:
 $f(w, x, y, z) = \sum m(0, 1, 5, 6, 7, 9, 13, 14)$ using multiplexer tree structure. The first level should consist of three 2-to-1 line multiplexer with a variable y on its select line. The second level should consist of a 4-to-1 line multiplexer circuit variables w and x on their select lines S_1 and S_0 respectively. 10
- b. Using the PAL device draw the logic diagram of a realization in PLD notation for the following set of Boolean functions. 10
- $$f_1(x, y, z) = \sum m(1, 2, 4, 5, 7)$$
- $$f_2(x, y, z) = \sum m(0, 1, 3, 5, 7).$$

UNIT - IV

- 7 a. Implement SR Latch operation. Write its logic symbol and function table. List the difference between a latch and a flip – flop. 10
- b. Explain the operation of gated D-latch. Write its logic symbol and function table. Which problem is eliminated in D-Latch as compared to SR and $\bar{S} \bar{R}$ latch? 10
- 8 a. Explain the operation of pulse triggered master slave JK flip flop with timing diagram. Write its excitation table. 10
- b. Analyze the working of positive edge triggered D flip flop with neat diagram and function table. 10

UNIT - V

- 9 a. What is a register? Explain the operation of 4-bit Serial-in-Parallel out and 4-bit Parallel-in-Serial out shift register using D flip flop. 10
- b. Design and implement synchronous mod-6 counter using clocked D flip flops. 10
- 10 a. Explain the addressing modes of 8086 microprocessor. 10
- b. Discuss in detail register organization and memory segmentation in 8086 microprocessor. 10

* * *