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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Fifth Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; Dec - 2017/Jan - 2018

Digital CMOS VLSI Design

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a. With the help of neat diagrams, explain the structure and operation of MOS (Metal Oxide Semiconductor) system. 7

b. Explain substrate Bias effect in MOSFET. 5

c. Calculate the threshold voltage V_{TO} at $V_{SB} = 0$, for polysilicon gate n-channel MOS transistor, with the following parameters; substrate doping density $N_A = 10^{16}$ cm^{-3}, polysilicon gate doping density $N_D = 2x10^{20}$ cm^{-3}, gate oxide thickness $t_{ox} = 500$ A°, and oxide-interface fixed charge density $N_A = 4x10^{10}$ cm^{-2}, $\varepsilon_{si} = 11.7\varepsilon_o$. 8

2 a. Analyze the channel length modulation in MOS transistor. 7

b. Analyze the junction capacitances with relevant equations. 7

c. Derive an equation for threshold voltage of a MOS transistor. 6

UNIT - II

3 a. Explain the concept of Noise Immunity and Noise margins with relevant equations and diagrams. 7

b. Distinguish between enhancement load nMOS inverter and depletion load nMOS inverter along with circuit diagram. 8

c. For depletion load nMOS inverter with $V_{DD} = 5$ V, $V_{TO,\ driver} = 1.0$ V, $V_{TO,\ load} = -3$ V,

$\left(W/L\right)_{driver} = 2$, $\left(W/L\right)_{load} = \frac{1}{3}$, $K'_{n\ driver} = K'_{n\ load} = 25\mu A/V^2$, $\gamma = 0.4V^{1/2}$, $\phi_F = -0.3V$, 5

Calculate V_{IL}

4 a. With the help of relevant equations and diagrams explain the operation of CMOS Inverter. 10

b. Calculate fall time τ_{fall} for a CMOS Inverter with a power supply voltage of $V_{OD} = 5$ V, use both the average – current method and the differential equation method output 10

$C_L = 1pF$, $\mu_n C_{OX} = 20\ \mu A/V^2$, $\left(W/L\right)_n = 10$, $V_{T,n} = 1.0$ V, $V_{90\%} = 4.5$ V, $V_{10\%} = 0.5$ V

Contd….2

UNIT - III

5	a.	Analyze Two-input CMOS NOR gate with relevant equations and diagram.	8
	b.	Design the CMOS logic circuit for the function, $Z = \overline{(D+E+A)(B+C)}$.	4
	c.	Analyze the bias conditions and operating regions of CMOS transmission gates.	8
6	a.	Analyze the behavior of Bistable elements.	7
	b.	Design the CMOS SR latch circuits using NOR2 gates.	7
	c.	Analyze the function of a NAND based Master-Slave flip-flop.	6

UNIT - IV

7	a.	Analyze the basic principles of pass transistor circuits with relevant equations for logic "1" transfer.	8
	b.	Design and sketch the Dynamic CMOS logic circuit for the Boolean function; Z = (AB + C) + (E + D).	4
	c.	Analyze the charge storage and charge leakage phenomenon at soft node in a CMOS network.	8
8	a.	Analyze the basic principle of operation of NP-Domino logic.	8
	b.	Design and sketch the domino CMOS logic circuit for the Boolean function Z = (A + B) + CD + (E + F).	4
	c.	Analyze the voltage Bootstrapping with relevant equations.	8

UNIT - V

9	a.	Analyze the operational characteristics of npn BJT using Ebers-moll model in; (i) Forward Active mode ii) Reverse Active mode.	10
	b.	Analyze the Latch up phenomena in CMOS inverter and guidelines for avoiding latch up in CMOS circuit.	10
10	a.	Analyze the ESD protection system in CMOS circuit with relevant example.	10
	b.	Discuss the process of on-chip clock generation and distribution in CMOS circuit.	10

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