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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Third Semester, B.E. - Electrical and Electronics Engineering

Semester End Examination; Dec - 2017/Jan - 2018

Digital Electronics

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a. With the help of circuit diagram, explain the working of, i) NAND ii) NOR iii) X-OR Gate. 8

b. Show that $(A+B)\left(\overline{AB}\right) = A \oplus B$ with logic diagram. 6

c. The waveforms A and B shown in Fig. 1.c are applied to a two input NAND gate. Determine the output waveform: 6

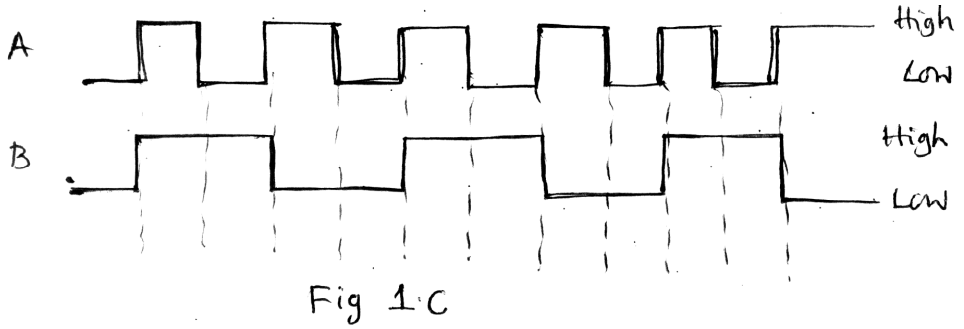

Fig 1.c

2 a. State and prove De Morgan's theorem. 8

b. Realize the XOR function using NOR logic only. 6

c. With examples, explain the SOP and POS standard forms to express Boolean function. 6

UNIT - II

3 a. F(A B C D) = Σm(1, 5, 6, 12, 13, 14) + d(2, 4) reduce by K-map and implement using NOR logic. 10

b. Distinguish between prime implicants and essential prime implicants. 4

c. Outline the basic Quine Mc-Cluskey procedure for simplifying a Boolean expression. 6

4 a. Design Half adder using NOR logic. 6

b. What is parallel binary adder? With example, demonstrate the working of binary adder. 6

c. With block diagram and truth table, explain the implementation of full subtrator. 8

UNIT - III

5 a. Design BCD to decimal decoder with use of decoder. 10

b. Explain the operation of basic SR Latch with NOR gates. 6

c. Convert JK flip-flop to T flip-flop. 4

Contd ... 2

6 a. Obtain the characteristic equation of :

i) JK flip-flop 8

ii) Edge triggered D flip-flop.

b. Implement the 4 to 1 line multiplexer with block diagram and function table. 8

c. Convert JK flip-flop to D flip-flop. 4

UNIT - IV

7 a. Distinguish between synchronous and asynchronous counters. 4

b. With a neat timing diagram, explain the working of serial-in-parallel-out shift register. 10

c. Explain the operation of Four-bit synchronous binary counter. 6

8 a. Explain the Mealy and Moore models of clocked synchronous sequential network. 10

b. Write a block diagram of a finite state model and explain. 6

c. Define;

i) State diagram ii) State tabel 4

iii) Transition tabel iv) Excitation tabel.

UNIT - V

9 a. Draw the schematic circuit and explain the operation of R-2R Ladder type DAC. 10

b. Draw and explain basic block diagram of a 4 bit successive approximation type ADC. 10

10 a. Draw and explain the operation of 3 bit Flash type A/D converter. 10

b. List the different types of Logic families circuits and compare them Emitter-coupled delay time. 5

c. Outline the characteristics of Emitter-Coupled Logic (ECL). 5

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