U.S.N | | | | | | | | | | |

P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Third Semester, B.E. - Information Science and Engineering

Semester End Examination; Dec - 2017/Jan - 2018

Digital Design

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1a. Obtain the prime implicants of the function : 10

$f(w,x,y,z) = \Sigma m(0,5,6,7,9,10,13,14,15)$

b. Simplify the following expressions : 10

(i) $(x+xy)(\bar{x}+y)+yz$ (ii) $\bar{w}\bar{z}\bar{y}+wz+\bar{y}z+xyz$

(iii) $F(A,B,C,D) = \Sigma m(7)+d(10,11,12,13,14,15)$.

2 a. Define combinational network. Explain with a block diagram. 5

b. Define logical gate. List out the universal gates and implement NAND gate using only NOR and X-OR gates. 12

c. Draw the synthesis of a gate combinational network for the following functions : 3

(i) $f(w,x,y,z) = \bar{w}x+\bar{x}(y+z)$ (ii) $f(w,x,y,z) = \bar{w}x+\bar{x}y+\bar{x}z$.

UNIT - II

3 a. Define decoder. Draw logic diagram of 3:8 decoder with enable input. 10

b. Discuss the parallel (ripple) binary adder with a suitable sketch. 10

4 a. Discuss the 4-bit carry lookahead adder with suitable sketch. 10

b. Realize a decoder of $f_1(x_2,x_1,x_0)_2 = \pi M(0,1,3,5)$ and $f_2(x_2,x_1,x_0)_2 = \pi M(1,3,6,7)$, 10

i) Using output OR-gates ii) Using output NOR-gates.

UNIT - III

5 a. Write short notes on the following with suitable examples : 10

i) ROM ii) PROMS iii) EPROMS.

b. What are the output voltages caused by each bit in a 5-bit ladder, if the input levels are 0 = 0 V and 1 = +10 V. 10

6 a. Discuss the 3-bit simultaneous A/D convertor using a logic diagram and using a 9318 priority encoder. 12

b. Discuss the concept of Dual-slope A/D converter with a suitable sketch. 8

Contd...2

UNIT - IV

7	a.	Differentiate between Pulse Triggered flip-flops versus Edge Triggered flip-flops with suitable examples. Explain the working of SR and JK flip-flops.	12
	b.	Discuss any two types of registers of your choice with suitable sketches.	8
8	a.	Discuss the following with suitable sketches : i) Ring counter ii) Johnson counter.	12
	b.	Discuss the various characteristics of ideal clock waveforms.	8

UNIT - V

9	a.	Show a method for constructing a 5 x 2 (Mod-10) decade counter.	12
	b.	Design the modulo-6 counter with corresponding state table and design equations with a suitable state diagram.	8
10	a.	Explain synchronous 3 bit up-down counter.	10
	b.	Discuss the concept of mod-8 parallel binary counter.	10

* * *