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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Third Semester, M. Tech - VLSI Design and Embedded System (MECE)

Semester End Examination; Dec - 2017/Jan - 2018

VLSI Testing and Verification

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a. Explain the process of realization of VLSI design along with the flow chart. 8

b. Obtain the expected and actual NOR gate output in the presence of assumed bridging faults. 6

c. Analyze the trends affecting testing in VLSI technology with respect to a speed testing and ATE cost. 6

2 a. Obtain the logic diagram for the functions $F = x_1x_2 + x_3x_4$ and find the boolean difference with respect to x_2. 6

b. Obtain CMOS schematic of 2 input NAND gate and analyze possible occurrence of breaks. 6

c. Explain Path Oriented Decision Making (PODEM) algorithm to generate test for combinational circuits. 8

UNIT - II

3 a. Define Ad-Hoc design rules for improving testability and explain with an example (Any one). 8

b. Apply Level Sensitive Scan Design (LSSD) concept to clocked hazard free latch. 6

c. Explain the concept of controllability and observability along with relevant logic diagram. 6

4 a. Explain the general representation of a Linear Feedback Shift Register (LFSR). 6

b. Along with the block diagram, explain the controllability and observability problem by making use of boundary scan cell. 6

c. Apply signature analysis for *n*-bit shift register and analyze its performance. 8

UNIT - III

5 a. Develop a test algorithm for RAM. 10

b. Analyze the test generation and Built In Self-Test (BIST) for embedded RAMs. 10

6 a. Explain the importance of verification with respect to VLSI process. 10

b. Explain formal verification and equivalent checking with an example. 10

UNIT - IV

7 a. Explain the role of verification and various levels of verifications. 8

b. Analyze Event-Driven simulation with an example. 6

c. List out the application of different levels of verifications. 6

Contd…2

8 a.	Mention the limitations of Linting tools and remedies for it.	6
b.	Write a note on simulations.	8
c.	Explain the cycle-based simulation with an example.	6

UNIT - V

9 a.	Explain the basic functionality of static trimming analysis. Mention the limitations.	12
b.	Explain the crosstalk delay analysis with an example.	8
10 a.	Explain Layout rule checks and electrical rule checks.	8
b.	Explain the cross talk glitch analysis with an example.	12

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