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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Third Semester, M.Tech. - VLSI Design and Embedded Systems (MECE)

Semester End Examination; Dec - 2017/Jan - 2018

Advances in VLSI Design

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a. Plot the conduction characteristics of an *n*-channel enhancement and *n*-channel depletion type MOS transistor. 6

b. Realize two input NAND gates using CMOS and Bi-CMOS logic. 6

c. With an aid of sketches of MESFET, explain the behavior of MESFET under different gate bias conditions ($V_g = 0$; V_{ds} = positive). 8

2 a. Explain the principles of modulation doping with help of band diagram. 6

b. Derive an expression for pinch-off voltage in a MESFET with an active layer thickness of '*t*'. 6

c. Draw the MODFET device structure consisting GaAs and ALGaAs - and explain its operation. 8

UNIT - II

3 a. With the aid of neat sketches of energy band diagrams, explain ideal *n*-type metal-insulator semiconductor device biased into Accumulation, Depletion and Inversion. 10

b. Derive an expression for cut-off frequency of a MOSFET using small signal equivalent circuit model. 6

c. Calculate the cut-off frequency of a MOSFET having the following data: L = 1μm; *n*-channel device with a P-type substrate; $\mu_n' = 1200$ cm^2/V$_s$; Z = 10 L; V_T = 1.1 V and V_G = 5 V. 4

4 a. Describe the various factors that alters MOSFET device performance due to short channel effect. 6

b. On applying the constant field scaling approach determines the scaled threshold voltage and drain current. Also prove that drain current scales linearly with dimensions and voltages. 8

c. Write a short note on processing challenges to further CMOS miniaturization. 6

UNIT - III

5 a. With an aid of a neat sketch, explain the construction and working of a carbon nanotube FET. Mention its advantages and disadvantages. 8

b. Sketch the SOI and bulk MOSFET structures and show the difference between them. 6

c. List out the advantages of molecular materials. 6

6 a. With the help of neat sketches, explain molecular structure of the molecular diode under; 8

i) Forward ii) Reverse bias.

Contd…2

b. Differentiate between Convention computing and Tactile Computing. 6

c. Describe how Teremac utilizes a fat-free architecture, which is immune to pathway interruptions. 6

UNIT - IV

7 a. With an aid of schematic and stick diagrams explain NMOS inverting and Non-inverting super buffers. 6

b. Derive an expression for minimum delay in terms of number of states and scale factor. 6

c. Realize a general two-variable functional block circuit to perform following functions using nMOS: 8

i) AND ii) NAND iii) OR

iv) NOR v) XOR vi) XNOR.

8 a. With an aid of a block diagram, differentiate between ratioed and Ratio-less dynamic logic circuits. 6

b. Find the total resistance, total capacitance and delay of a 3 mm long poly silicon line of width 3 μm = 2 λ, resistance 50 Ω/sq and capacitance 0.04 f F/μm^2 = 0.36 f F/sq. Also, find improved performance if one, two, three inverters of ratio 8 to 1 are inserted in the line. (Assume each inverter has a delay t_I = 1ns when diving a line of 1mm long; Neglect delay changes with driving resistance). 8

c. Realize two input NAND and NOR gates using nMOS pass transistor logic. 6

UNIT - V

9 a. With an aid of a conceptual logout, design a stick diagram of a 3 input tally circuit using pass transistor show all the combinations of inputs and paths activated using truth table. 10

b. Using FET switches, explain Barrel shifter operation which performs 4 shifts. Draw the supporting diagram. 10

10 a. Describe the following techniques which are used to reduce complexity of IC design: 8

i) Hierarchy ii) Regularity iii) Modularity iv) Locality.

b. Realize following expressions using PLA: 6

$Y_1 = x_0 + x_1, \qquad Y_2 = x_0\overline{x}_1 + \overline{x}_0 x_2 + x_1$

c. Write short notes on: 6

i) Standard cell based design ii) Full Custom design.

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