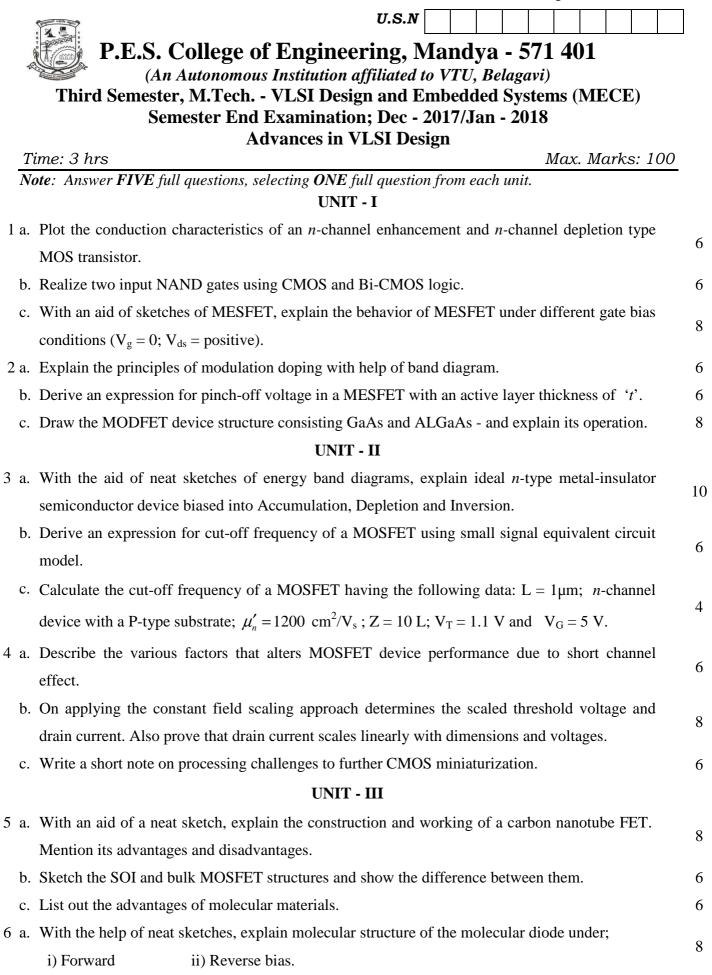
Page No... 1



P	15MECE332	Page No 2	
b.	b. Differentiate between Convention computing and Tactile Computing.		
c.	Describe how Teremac utilizes a fat-free a	rchitecture, which is immune to pathway	ć
	interruptions.		6
UNIT - IV			
7 a.	a. With an aid of schematic and stick diagrams explain NMOS inverting and Non-inverting super		
	buffers.		
b.	. Derive an expression for minimum delay in terms of number of states and scale factor.		
c.	c. Realize a general two-variable functional block circuit to perform following functions using		
	nMOS:		8
	i) AND ii) NAND	iii) OR	0
	iv) NOR v) XOR	vi) XNOR.	
8 a.	a. With an aid of a block diagram, differentiate between ratioed and Ratio-less dynamic logic		
	circuits.		
b.	b. Find the total resistance, total capacitance and delay of a 3 mm long poly silicon line of width		
	3 $\mu$ m = 2 $\lambda$ , resistance 50 $\Omega$ /sq and capacitance 0.04 <i>f</i> F/ $\mu$ m <sup>2</sup> = 0.36 <i>f</i> F/sq. Also, find improved		
	performance if one, two, three inverters of ratio 8 to 1 are inserted in the line. (Assume each		
	inverter has a delay $t_I = 1$ ns when diving a line of 1mm long; Neglect delay changes with		
driving resistance).			
c.	c. Realize two input NAND and NOR gates using nMOS pass transistor logic.		
UNIT - V			
9 a.	9 a. With an aid of a conceptual logout, design a stick diagram of a 3 input tally circuit using pass transistor show all the combinations of inputs and paths activated using truth table.		
b.	b. Using FET switches, explain Barrel shifter operation which performs 4 shifts. Draw the		
	supporting diagram.		
10 a	10 a. Describe the following techniques which are used to reduce complexity of IC design:		
	i) Hierarchy ii) Regularity iii) M	odularity iv) Locality.	8
b.	b. Realize following expressions using PLA:		
	$Y_1 = x_0 + x_1,$ $Y_2 = x_0 \overline{x_1} + \overline{x_0} x_2 + x_1$		
c. Write short notes on:			~
	i) Standard cell based design ii) Full G	Custom design.	6

\* \* \*