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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Sixth Semester, B.E. - Computer Science and Engineering

Semester End Examination; June - 2017

Advanced Computer Architecture

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1. a. Bring out the difference between;
   i) Explicit and Implicit parallelism ii) UMA and NUMA
   iii) Multiprocessor and multicomputer iv) SIMD and MIMD. 8

   b. With a figure, explain vector supercomputer. 8

   c. Consider the execution of an object code with 200,000 instructions on a 40 MHz processor. The program consists of four major types of instructions. The instruction mix and the number of cycles (CPI) needed for each instruction type is given below based on the result of a program trace experiment.

Instruction type	CPI	Instruction mix
Arithmetic and logic	1	60%
Load/store cache hit	2	18%
Branch	4	12%
Memory reference with cache miss	8	10%

   4

   (i) Calculate the average CPI when the program is executed on a uniprocessor with the above trace.

   (ii) Calculate the corresponding. MIPS rate based on the CPI obtained in part (i).

2 a. With an example, discuss mismatch between software and hardware parallelism. 8

   b. Compare control flow and data flow computers. 6

   c. Find the node degree, network diameter and number of links for the static interconnection networks - Binary tree, torus, star, and hypercube. 6

UNIT - II

3 a. Explain VLIW processors. 10

   b. With neat diagram, briefly explain the Backplane bus system. 5

   c. List five differences between CISC and RISC computers. 5

4 a. With suitable figure, show that high and low order interleaving can be combined to yield a memory system with increased bandwidth and fault tolerance. 10

Contd….2

b. Briefly explain two methods of memory interleaving. Also indicate when each is preferred over the other. 10

UNIT - III

5 a. Consider the below reservation table :

	1	2	3	4
S1	X			X
S2		X		
S3			X	

8

(i) What are the forbidden latencies (ii) Draw state transition diagram

(iii) List all simple cycles and greedy cycles

(iv) Find optimal constant latency cycle and minimal average latency

(v) Let pipeline clock period be 20 ns, find throughput of the pipeline.

b. Explain any two mechanisms for instruction pipelining. 6

c. Explain static arithmetic pipeline. 6

6. a Why branch instructions are hazardous to pipeline design. Briefly explain one static and one dynamic branch prediction method. 8

b. Explain Tomasulo's algorithm for dynamic instruction scheduling. 7

c. Derive the formula to find the speed up of k-staged pipeline. What is the maximum speedup possible? 5

UNIT - IV

7 a. What is cache coherence problem? Give the basic idea behind snoopy cache coherence protocol. Draw the state transition diagram of write-invalidate write-through snoopy protocol. 7

b. Explain how atomic operation Fetch and Add can be used to overcome Hot spot problem. 7

c. With a diagram, explain schematic design of a cross point switch. 6

8 a. Mention drawback of snoopy cache coherence protocol. How it is overcome by a directory based protocol. Describe any one method of implementing directory based protocol. 8

b. Explain any two methods to control smooth network traffic without causing congestion or deadlock situation. 8

c. Explain virtual channel. 4

UNIT - V

9 a. Briefly explain how "Evolution of Galaxies" Problem can be parallelized. 10

b. Explain all the steps in a parallelization process. 10

10a. Explain the orchestration of "Equation solver" problem under data parallel model. Also write its pseudo code. 10

b. Explain cost scaling and physical scaling. 10

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