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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Sixth Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; June - 2017

Digital Design using Verilog HDL

Time: 3 hrs *Max. Marks: 100*

*Note: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1. a List the value level and strength level of logical variable used in verilog. 8
   b. Explain the different system tasks with examples. 6
   c. Design and develop a verilog code for SR Latch using gate level modeling. 6
2. a. Design the 4:1 multiplexer by using if and else statement. 8
   b. Explain with an example how the ports can be connected to external signal. 6
   c. Explain the different operator types and symbols provided in verilog. 6

UNIT - II

3. a. Explain the initial and always blocking statements with an example each. 8
   b. Define blocking and non blocking statements. Illustrate with examples. 6
   c. Illustrate with an example each sequential and parallel blocks. 6
4. a. Mention the differences between task and functions. 8
   b. Explain the use of keywords ‘assign’ and ‘deassign’ with examples. 6
   c. Develop a verilog model for the given functions. 6
   i) a ii) a+b iii) a-b iv) a/b v) a<<1 vi) a>>1 vii) a>b

UNIT - III

5. a. Briefly describe the different types of delay models with examples. 6
   b. With the help of flow diagram explain the various steps involved in back annotation. 6
   c. Write the symbol of bidirectional switches and mention how the delay specification takes place in MOS and CMOS switches. 8
6. a List the User defined primitives (UDP) rules of verilog language. 6
   b. Write a verilog stimulus of 4:1 multiplexer with UDP. 6
   c. With the knowledge of UDP, illustrate the working of T flip flop. 8

UNIT - IV

7. a. Discuss the different steps involved in programming language interface (PLI). 8
   b. Write the consumer routine for Value Change Link (VCL). 6
   c. List and explain the PLI Library routines. 6

Contd….2

8	a.	Briefly explain the impact of logical synthesis.	6
	b.	Explain the design flow of 'RTL to gate level' description.	6
	c.	Explain the different verilog HDL operators for logic synthesis.	8

UNIT - V

9	a.	With the help of RTL description draw the finite state machine for news paper vending machine.	10
	b.	Explain the traditional verification flow in verilog.	10
10	a.	Explain in detail the architectural model.	6
	b.	Explain hardware acceleration.	8
	c.	Discuss the formal verification flow.	6

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