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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Second Semester, M. Tech – VLSI Design and Embedded System (MECE)

Semester End Examination; June - 2017

Design of Analog and Mixed Mode VLSI Circuits

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a. Discuss the important aspects of MOSFET-model and hence, construct the complete circuit model of a MOSFET for small signal operation, considering device capacitances, channel length modulation and body effect. 8

b. Describe the operation of source follower with MOSFET as current source load, both by excluding and including body effect. 7

c. For the common gate MOSFET amplifier with resistive load R_D, prove that $\frac{\partial V_{out}}{\partial V_{in}} = g_m(1+\eta)R_D$ with the usual notations. Draw the input-output characteristics. 5

2 a. Draw the cascode stage circuit and its equivalent circuit as well as input-output characteristics, and discuss the operation and hence, show the extension of cascade structure to two or more devices to get higher output impedance. 12

b. Sketch the separate circuits of folded cascode with biasing and N-MOSFET input and describe their operations. 8

UNIT - II

3 a. For a MOS differential pair circuit with two separate inputs, derive the expression for differential drain current $\left(I_{D_1} - I_{D_2}\right)$. 8

b. Sketch the circuit diagram of differential pair sensing CM-input and develop the expression for common mode to differential mode conversion $A_{CM\text{-}DM}$. 12

4 a. How is cascode current mirror realized using cascode current source? Describe with the help of circuit diagrams. 8

b. Draw a MOS differential pair circuit with active current-mirror sensing a common mode change and develop the expression for CMRR. 12

UNIT - III

5 a. Sketch the circuit of source follower with output capacitance and its corresponding high frequency equivalent circuit and derive the expression for the transfer function. 10

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b. Draw the source follower circuit showing noise sources and derive the expression for the input-referred raise voltage. 10

6 a. Neglecting the body effect ($\gamma = 0$), calculate the transfer function (V_{out} / V_{in}) for the simplified cascode stage shown in Fig. Q 6(a).

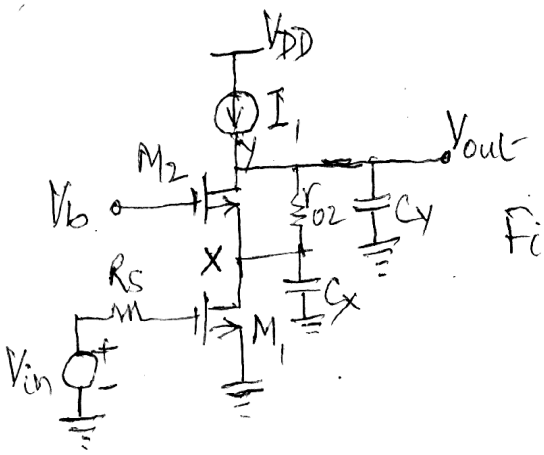

Fig Q6(a) Simplified cascode stage at high frequencies. 10

b. Show that the input noise voltage squared of differential pair is twice the input noise voltage squared of a common-source stage for a differential pair circuit including input-referred noise sources. 10

UNIT - IV

7 a. Sketch the circuit implementation of a two-stage OP-AMP and describe the functions of each stage. 6

b. Discuss the various methods of boosting the gain in differential cascode. 6

c. Discuss the response of a linear OP-AMP to a step input and derive the expression for the output voltage. Draw the relavant circuit diagram and the corresponding waveforms. 8

8 a. For a two-stage OP-AMP, derive the expression for the input-referred thermal noise voltage. 10

b. For a differential pair with active current mirror load and capacitive feedback, develop the expression for low frequency PSRR. 10

UNIT - V

9 a. Explain the basic principles of VCO and the seven important performance parameters. 10

b. Sketch the cross-coupled oscillator circuit with tail current source and explain how the problems of conventional oscillators are overcome? 10

10 a. Describe the problem of lock acquisition and its solution in type-I PLL. 7

b. With circuit diagram, explain the methods to establish supply independent currents in order to realise current references. 8

c. Explain the techniques to derive the temperature independent references. 5

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