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P.E.S. College of Engineering, Mandya - 571 401
(An Autonomous Institution affiliated to VTU, Belagavi)
Second Semester, M. Tech - VLSI Design and Embedded System (MECE)
Semester End Examination; June - 2017
Low Power VLSI Design

Time: 3 hrs   *Max. Marks: 100*

*Note: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a.	Briefly discuss the static and dynamic power dissipation in CMOS circuits.	8
b.	Show that the short circuit power dissipation of an encoded inverter is $$P_{SC} = \frac{\beta}{12}\left(V_{DD} - V_T\right)^3 \frac{\tau}{T}.$$	9
c.	What is meant by overlap capacitance? Give its equation.	3
2 a.	Discuss the impact of technology scaling and innovation trends for low power devices.	10
b.	What are the problems associated with transistor and gate sizing for dynamic power reduction?	4
c.	Explain the important components of diffusion capacitance with necessary equations.	6

UNIT - II

3 a.	Discuss the following gate level logic simulation : i) Internal switching energy ii) Gate level capacitance estimation.	10
b.	Discuss the power models based on activities.	8
c.	What are the fundamental issues in composing a power model?	2
4 a.	Bring out the differences between positive and negative correlation.	6
b.	Define Monte Carlo simulation process and also derivre the expression for minimum number of sampes 'N' by using Monte Carlo concept.	10
c.	The standard deviation of the power samples measured from a circuit has been observed to have ±20% fluctuations from the near. How many samples are required to have 99% confidence that the error of sample mean is within ±5% ? Given $Z_{\alpha/2} = 2.58$.	4

UNIT - III

5 a.	Derive the expression for average frequency 'F' of the circuit related to entropy of the signals.	10
b.	Compute the transition density and static probability of $y = ab+c$ given p(a) = 0.2, p(b) = 0.3, p(c) = 0.4, D(a) = 1, D(b) = 2 and D(c) = 3.	10

6 a.	Briefly discuss the low power digital cell library.	8
b.	Explain the concept of glitches by considering CMOS XOR gate circuit.	6
c.	Discuss the low voltge swing circuit techniques.	6

UNIT - IV

7 a.	Explain gate reorganization with necessary diagrams.	10
b.	Explain the architecture of bus invert encoding along with relevant diagrams.	10
8 a.	Explain adaptive filtering with necessary diagrams.	10
b.	Discuss the concept of parallel architecture with voltage reduction.	10

UNIT - V

9 a.	Explain how to insert buffer in clock tree with example.	10
b.	Derive the expression for tolerable skew.	10
10 a.	Explain the algorithmic load analysis and optimization.	10
b.	Briefly discuss the architecture level estimation and synthesis.	10

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