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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Second Semester, M. Tech - VLSI Design and Embedded System (MECE)

Semester End Examination; June - 2017

Design of VLSI Systems

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a.	Explain briefly the digital design domain and levels of abstraction with the help of Y chart.	6
b.	What is hierarchy? Explain with a difference engine as an example.	6
c.	With neat diagram, explain the Xilinx FPGA architecture and configurable logic blocks.	8
2 a.	What is logic optimization? Explain with a typical flow diagram.	10
b.	Discuss different EDA tools which are used in VLSI design.	10

UNIT - II

3 a.	Describe briefly the different design capture tools used in VLSI design.	12
b.	Explain the following : i) Network isomorphism ii) Layout extraction iii) Back annotation.	8
4 a.	Draw a carry chain adder constructed using propagate, generate and kill signals.	6
b.	With a necessary diagram, explain the Manchester adder with carry skip.	6
c.	With the help of a neat diagram, explain the unsigned magnitude comparator.	8

UNIT - III

5 a.	Explain how multiplication is performed using radix 4 booth encoding.	12
b.	Explain array funnel shiffer with a neat diagram.	8
6 a.	Explain the read and write operation with respect to SRAM.	8
b.	Draw the basic ROM architecture using NOR array and explain its working.	8
c.	Explain briefly quesues in memory.	4

UNIT - IV

7 a.	Explain the FSM design procedure with an example.	10
b.	What are the properties of I/O subsystem?	10
8 a.	How global clock is generated? Explain if with respect to PLL.	10
b.	List the properties of ideal power distribution network and explain IR drop and $\alpha \frac{di}{dt}$ noise.	10

UNIT - V

9 a.	Explain the following : i) Non recurring engineering costs ii) Recurring engineering costs iii) Fixed costs.	10
b.	With the help of a neat diagram, explain boundary scan architecture.	10
10.	Write a short notes on : i) Design for testability ii) Stuck at faults iii) Observability and Controllability.	20

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