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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Third Semester, B.E. - Computer Science and Engineering

Semester End Examination; Dec - 2016/Jan - 2017

Digital Logic Design

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a. Explain with examples ;
i) Positive and Negative logic
ii) NOR as universal gate
iii) NAND as universal gate. — 10

b. Design a minimum hardware circuit for the Boolean expression using QM technique, $f(w, x, y, z) = \sum m(0, 5, 6, 7, 9, 10, 13, 14, 15)$. — 10

2 a. Explain with examples;
i) De-Morgan's theorem
ii) Principle of Duality
iii) Consensuses theorem. — 10

b. Consider a circuit with 4 variables input A, B, C, D and one output 'Z'. Output Z = 1 if B or C is high, but not both. And also Z = 1, if all input is same. Design a minimum hardware circuit using K-map. — 10

UNIT - II

3 a. Mention the building blocks of arithmetic circuits explain the same with examples. — 10

b. Implement the following expression using 4 : 1 MUX and 8 : 1 MUX, $f(A, B, C, D) = \Sigma m(0, 1, 5, 6, 7, 8, 9, 10, 15)$. — 10

4 a. Explain:
i) 4 : 1 MUX
ii) 2-bit magnitude comparator. — 10

b. Implement the following using 3 : 8 decoder,
$f_1(A, B, C) = \Sigma m(1, 3, 4, 5)$
$f_2(A, B, C) = \Sigma m (0, 2, 5, 6, 7)$
$f_3(A, B, C) = \Sigma m(1, 2, 3, 6)$ — 5

c. Design a 6-bit odd parity generator. — 5

Contd.....2

UNIT - III

5	a.	Differentiate between PLA and PAL.	5
	b.	Explain edge triggered SR Flip-Flop.	5
	c.	Giving characteristic equations, state diagram and excitation fable of JK and D Flip-Flop, convert D Flip-Flop to JK Flip-Flop.	10
6	a.	Explain JK Flip-Flop.	5
	b.	Implement the following using PLA, $f_1(A, B, C) = \Sigma m\ (0, 2, 3, 7)$ $f_2(A, B, C) = \Sigma m\ (1, 2, 4, 5)$ $f_3(A, B, C) = \Sigma m(1, 3, 5, 6, 7)$	5
	c.	Convert SR Flip-Flop to T Flip-Flop, giving characteristic equation, excitation table and state diagram of SR Flip-Flop and T Flip-Flop.	10

UNIT - IV

7	a.	Giving circuit diagram, truth table and wave diagram, explain SIPO shift register (4-bit).	10
	b.	Design a counter using JK flip flop that counts as, $2\rightarrow1\rightarrow0\rightarrow3\rightarrow5\rightarrow6\rightarrow4\rightarrow\ldots.$	10
8	a.	Briefly explain the different applications of shift register.	10
	b.	Using T Flip-Flops design a synchronous counter that counts in the following sequence, $0\rightarrow1\rightarrow2\rightarrow3\rightarrow4\rightarrow5\rightarrow6\rightarrow7\rightarrow0\ldots.$	10

UNIT - V

9	a.	Briefly explain : i) Binary ladder ii) A/D counter method conversion.	10
	b.	Write Verilog/VHDL code to implement 3 : 8 decoder.	5
	c.	Write Verilog/VHDL code to implement Johnson counter.	5
10	a.	Explain the different A/D techniques.	10
	b.	Write Verilog / VHDL code to implement 8:1 MUX.	5
	c.	Write Verilog / VHDL code to implement 3-bit up counter and down counter.	5

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