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	U.S.N		
P.E.S. College of Engineering, Mandya - 571 401 (An Autonomous Institution affiliated to VTU, Belgaum) Third Semester, B.E Computer Science and Engineering Semester End Examination; Dec - 2016/Jan - 2017 Computer Organization			
Tin	ne: 3 hrs Max. Marks: 100		
Not	e: Answer FIVE full questions, selecting ONE full question from each unit.		
	UNIT - I		
1 a.	Explain the various types of computers.	5	
b.	Explain the three systems used for representing numbers with examples.	5	
c.	Explain how performance is affected by technology and parallelism?	6	
d.	Convert the decimal numbers 7 and 13 to 5 bit 2's complement numbers and perform addition.	4	
2 a.	Explain Big-endian and Little-endian methods with examples.	5	
b.	Explain basic instruction types.	5	
c.	What is an addressing mode? List and explain the various addressing modes.	10	
	UNIT - II		
3 a.	What is subroutine nesting? Explain the role of processor stack while nesting.	5	
b.	What is the basic technique of accessing an I/O device? What are its limitations?	5	
c.	How multiple devices are handled in processing interrupts? Explain vectored interrupts in details.	10	
4 a.	Describe the interaction between assembly language and 'C' language.	10	
b.	Explain various types of parameter passing with examples.	10	
	UNIT - III		
5 a.	With a neat sketch, explain single bus organization of the data path inside a processor. Further, list and explain the generic operations performed during instruction executions.	10	
b.	With neat sketches, explain hardwired control (Control unit, decoding-encoding logic).	10	
6 a.	What is bus arbitration? Explain simple arrangements for the same.	5	
b.	Explain in detail PCI bus.	10	
c.	Explain synchronous BUS operation.	5	
	UNIT - IV		
7 a.	With a neat sketch, explain the organization of a 2m X 32 memory using 512 K x 8 static memory chips.	6	
b.	Explain various forms of ROM.	4	
c.	Write a note on DMA	5	
d.	What is page replacement? With an example explain any one algorithm.	5	

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8 a.	Explain the three types of cache mapping. Give suitable examples.	10
b.	Explain hit rate and miss penalty.	5
c.	With a block diagram, explain virtual memory organizations.	5
	UNIT - V	
9 a.	With diagram, explain binary addition/subtraction logic network.	5
b.	What is fast adder? Explain it's logic.	5
c.	Explain the process of mutiplication of positive numbers with a registers configuration and an illustration.	10
10 a.	What is bit-pair recoding of multiplier? Explain its benefit with an example.	5
b.	Write the circuit for a binary division. Illustrate how it works, taking an example.	10
c.	Explain single and double precision IEEE floating point presentations of numbers.	5

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