## P.E.S. College of Engineering, Mandy - 571401

(An Autonomous Institution affiliated to VTU, Belgaum)
First Semester, B.E. - Semester End Examination; Dec - 2016/ Jan - 2017
Electronic Devices and Communication
(Common to all Branches)
Time: 3 hrs
Max. Marks: 100
Note: Answer FIVE full questions, selecting ONE full question from each unit.

## UNIT - I

1 a. Calculate load Voltage $\left(\mathrm{V}_{\mathrm{L}}\right)$ and load current $\left(\mathrm{I}_{\mathrm{L}}\right)$ for the series diode configuration shown in Fig. Q1(b). Also plot the d.c. load line and mark the Q-point on it.

$$
\begin{equation*}
E=10 \mathrm{~V} \frac{ \pm}{-[ } \quad-V_{D}=0.7 \mathrm{~V}, R_{L}=0.5 \mathrm{k} \Omega \tag{5}
\end{equation*}
$$ and related waveforms.

c. Calculate the following for the network shown in Fig. Q1(c) :
(i) Range of $\mathrm{R}_{\mathrm{L}}$ and $\mathrm{I}_{\mathrm{L}}$ that will result in $\mathrm{V}_{\mathrm{RL}}$ being maintained at 10 V .
(ii) Determine the maximum wattage rating of the diode.
(iii) If zener maximum wattage is increased to 380 mW , what is the new value of $\mathrm{I}_{\mathrm{L} \text { min }}$ ?


## Figure \& 1(c)

2 a. Write short notes on the following :
i) Photodiodes
ii) Solar cells.
b. Explain the principle of LCD (Liquid Crystal Display).
c. Calculate $V_{0}, V_{1}, I_{D 1}$ and $I_{D 2}$ for the parallel diode configuration shown in Fig. Q2(b)


Figure Q $2(b)$.
UNIT - II
3 a. Describe the basic operation and characteristics of $n$-channel depletion type MOSFET.
b. Explain the use of the complementary arrangement of CMOS inverter with figure.
c. Sketch the transfer characteristics for an $n$-channel enhancement-type MOSFET from the drain characteristics.

4 a. Define Barkhausen criterion for oscillation. Explain the feedback circuit that is used as an oscillator.
b. Sketch the E-MOSFET voltage divider configuration and its AC equivalent network.
c. Write circuit of FET phase shift oscillation and explain its working.

## UNIT - III

5 a. Derive equation for output voltage of an Op-Amp circuits,
i) Inverting Amplifier
ii) Summing Amplifier
iii) Differentiator Circuit.
b. Define the Op-Amp frequency parameters :
i) Gain Bandwidth
ii) Slew rate (SR)
iii) Maximum signal frequency.
c. Calculate the output voltage of an Op-Amp for input voltages of $\mathrm{Vi}_{1}=150 \mu \mathrm{~V}$ and $\mathrm{Vi}_{2}=140 \mu \mathrm{~V}$. The amplifier has a differential gain of $\mathrm{A}_{\mathrm{d}}=4000$ and the value of CMRR is,
i) 100
ii) $10^{5}$.

6 a. Show the connection of three Op-Amp stages to provide outputs that are $-10,-20$ and -50 times larger than the input. Use a feedback resistor $\mathrm{R}_{\mathrm{f}}=500 \mathrm{k} \Omega$ in all stages.
b. Explain the use of active low pass and high pass filter with circuit and ideal response of filters.
c. Calculate the output voltage of an Op-Amp inverting amplifier with a sinusoidal input of $2.5 \mathrm{mV}, \mathrm{R}_{\mathrm{f}}=200 \mathrm{k} \Omega$ and $\mathrm{R}_{1}=2 \mathrm{k} \Omega$.

## UNIT - IV

7 a. Write the block diagram of a microcontroller and explain each block.
b. Compute:
i) $1101.1011_{(2)}=$ $\qquad$ (10) $=$ $\qquad$ (16)
ii) $3 \mathrm{E} \cdot 4 \mathrm{FC}_{(16)}=$ $\qquad$ (10) $=$ $\qquad$
P13EC15
iii) Perform Binary addition 95
$+189$
iv) Perform Binary subtraction
189
-95
8 a. Write PSW (Program Status Word) of 8051 and explain use of each bit in it. ..... 8
b. Explain internal RAM organization of 8051 microcontroller with figure. ..... 12
UNIT - V
9 a. Define the following terms in wireless communication :
i) Base stationii) Mobile stationiii) Simple and Duplex communication.
b. Describe the call handling procedure from mobile to wire line with block diagram. ..... 10
c. Explain handoff procedure in mobile communication. ..... 4
10 a. Describe the Infrastructure and Ad-hoc network topology with diagrams. ..... 10
b. Explain the GSM architecture with block diagram. ..... 10

