



## P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

**Third Semester, B.E. - Electronics and Communication Engineering**  
**Semester End Examination; Dec - 2016/Jan - 2017**

### FET and Op-Amp Circuits

Time: 3 hrs

Max. Marks: 100

**Note:** i) Answer **FIVE** full Questions, selecting **ONE** full question from each unit.

ii) Assume suitable missing data, if any.

#### UNIT - I

- 1 a. Explain the formation of channel for current flow in NMOS transistor. Also determine the total capacitance between gate and the channel. 8
- b. Sketch the transfer characteristics of NMOSFET. Describe the MOSFET as an amplifier and as a switch. 6
- c. An NMOS transistor has  $\mu_n C_{ox} = 60 \mu A/V^2$ ,  $\frac{W}{L} = 40$ ,  $V_t = 1 V$  and  $V_A = 15 V$ . Find  $g_m$  and  $r_o$  when, (i) The bias voltage  $V_{GS} = 1.5 V$  and when (ii) The bias current  $I_D = 0.5 mA$ . 6
- 2 a. Describe the development of the  $T$  equivalent circuit model for the MOSFET. 9
- b. Explain the frequency response of the common source amplifier. 11

#### UNIT - II

- 3 a. Define the following Op-Amp parameters: 4
- (i) CMRR (ii) PSRR
- (iii) Input Offset Voltage (iv) Slew rate.
- b. Using a 741 Op-Amp, design a non-inverting amplifier to have a voltage gain of 66. The input signal is 15 mV. 8
- c. Sketch a two-input Op-Amp inverting summing circuit. Derive an equation for the output voltage in terms of the input. 8
- 4 a. Write the circuit diagram for differential input/output amplifier. Derive the equation for closed-loop voltage gain. 7
- b. Design a capacitor-coupled voltage follower using a 741 Op-Amp. The lower cut off frequency for the circuit is to be 50 Hz and the load resistance is 3.9 k $\Omega$ . 7
- c. Describe the circuit operation of capacitor-coupled non-inverting amplifier. 6

#### UNIT - III

- 5 a. Explain how the upper cutoff frequency can be set for inverting amplifier? 6
- b. Sketch the capacitor-coupled voltage follower using a single-polarity supply. Briefly explain. 7

- c. Show how feedback in an Op-Amp inverting amplifier can produce instability and explain the conditions necessary for oscillations to occur in an Op-Amp circuit. 7
6. a. Explain the miller effect compensation. 7
- b. List precautions that should be observed for Op-Amp circuit stability. 7
- c. Write the circuit of a current source for a floating load and the circuit operation. 6

#### UNIT - IV

- 7 a. Sketch the diagram for an Op-Amp differentiating circuit. Explain. 6
- b. Design a non saturating precision half-wave rectifier to produce a 2 V peak output from a 1 MHz sine wave input with a 0.5 V peak value. Use a Op-Amp with a supply voltage of  $\pm 15$  V. 6
- c. Write the Op-Amp Zener diode peak clipper circuit. Explain its operation. 8
- 8 a. Sketch an Op-Amp precision clamping circuit, draw the input and output waveform and explain the circuit operation. 10
- b. Write the diagram for an Op-Amp sample and hold circuit. Sketch the signal, control and output voltage waveforms. Explain the circuit operation. 10

#### UNIT - V

- 9 a. Sketch the circuit diagram of an Op-Amp Wein bridge oscillator. Write the oscillator waveforms and explain the circuit operation. 10
- b. Write the circuit diagram, gain frequency response and phase frequency response of a second order low-pass filter. Explain its operation. 10
- 10a. An unregulated DC power supply output changes from 20 V to 19.7 V when the load is increased from zero to maximum. The voltage also increases from 20 V to 20.2 V when the AC supply increases by 10%. Calculate the load and source effects and the load and line regulations. 6
- b. Show how the output voltage of an Op-Amp series regulator may be made adjustable. Explain. 7
- c. Sketch the basic circuit of a 723 IC voltage regulator. Briefly explain. 7

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