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# P.E.S. College of Engineering, Mandya - 571 401

***(An Autonomous Institution affiliated to VTU, Belgaum)***

**Fifth Semester, B.E. - Electronics and Communication Engineering**

**Semester End Examination; Dec - 2016/ Jan - 2017**

**Digital CMOS VLSI Design**

*Time: 3 hrs* *Max. Marks: 100*

***Note**: i) Answer **FIVE** full questions, selecting **ONE** full question from each unit.*
*ii) Missing data, if any, may be suitably assumed.*

**UNIT - I**

1 a. Calculate the threshold voltage $V_{TO}$ for $V_{SB}=0$, given substrate loping $10^{15}/cc$, poly silicon gate doping density $10^{20}/cc$, gate oxide thickness $650\,\mathring{A}$, $N_{ox}=2\times10^{10}/cm^2$, $\varepsilon_{Si}=11.7\varepsilon_0$, $\varepsilon_{ox}=3.97\varepsilon_0$. — 12

b. Analyze the input of second order effects with respect to;
(i) Substrate bias effect (ii) Channel length modulator. — 8

2 a. Draw the layout of resistive load inverter with diffused resistor and undoped poly silicon resistor. — 4

b. Analyze the VTC of 3 CMOS invertors with different $\frac{\beta n}{\beta P}$. — 4

c. Calculate the noise margins of CMOS inverter. Given $V_{DD}=3.3V$, $V_{TO,n}=0.6$, $V_{TP}=-0.7V$, $K_n=200\mu A/V^2$, $K_p=80\mu A/V^2$. — 12

**UNIT - II**

3 a. Derive an expression for $\tau_{PLH}$ and $\tau_{PLH}$ of CMOS inverter considering;
(i) $V_{50\%}$ (ii) $V_{10\%}$ (iii) $V_{90\%}$ along with I/o w/f. — 10

b. Briefly analyze the influence of fringing electric fields upon the parasitic wire capacitance. — 4

c. Along with voltage and current waveform, obtain an expression for average power in CMOS inverter. — 6

4 a. Analyse the impact of interconnect delay over gate delay in sub-micron CMOS technology. — 6

b. Obtain an expression for delay by considering Elmore delay concept in a general RC tree network. — 8

c. With a typical voltages waveform, obtain an expression for oscillation frequency in a 3-stage ring oscillator. — 6

Contd….2

**UNIT - III**

5 a. Obtain an expression for switching threshold voltage of CMOS $NOR_2$ Gate. 6

b. Realize the function $F = AB\overline{C} + \overline{A}B + A\overline{C}$ using CMOS TG (transmission gates). 4

c. Obtain the Euler path and draw the optimized stick diagram for the function, $F = \overline{A(D+E)+BC}$. 10

6 a. Along with CMOS schematic and waveform, explain the working of NOR based clocked SR latch. 8

b. Along with gate level schematic, nMOS schematic and waveform explain the working of NAND based SR latch. 8

c. Realize the schematic of CMOS D latch version 1. 4

**UNIT - IV**

7 a. Discuss the charge storage and charge leakage phenomenon at a soft node in a CMOS n/w. 8

b. Analyze the working of high performance of DOMINO CMOS logic. In what way it is better than Dynamic CMOS logic? Explain. 12

8 a. Explain the voltage boot strapping principle. Hence derive an expression for $C_{boot}/C_S$. 8

b. Analyze the performance of NORA CMOS logic and obtain pipelined architecture using NORA CMOS logic. 12

**UNIT - V**

9 a. Derive an expression for $I_C$ in forward Active mode, using Ebers-moll equivalent circuit. 10

b. Realize the schematic of BiCMOS, NAND3 gate. 4

c. Discuss the H-tree and Buffered clock distribution n/w. 6

10 a. Analyze the response of delay V/s $C_L$ for CMOS and BiCMOS technology. 5

b. Discus briefly $L\left(di/dt\right)$ noise effect in output circuits. 6

c. Analyze the performance of 3 clock generation n/ws. 9

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