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P.E.S. College of Engineering, Mandya - 571 401
(An Autonomous Institution affiliated to VTU, Belgaum)
Seventh Semester, B.E. - Electronics and Communication Engineering
Semester End Examination; Dec - 2016/Jan - 2017
Low Power VLSI Design

Time: 3 hrs *Max. Marks: 100*

Note: Answer **FIVE** full questions, selecting **ONE** full question from each unit.

UNIT - I

1 a. Briefly analyze the parameters which are to be considered while designing for low power. 8

 b. Analyze the impact of sub threshold current and the sub threshold swing in long channel MOSFET. 6

 c. Explain the three basic principles that have fundamental limits on low power design. 6

2 a. Analyze the body effect along with mathematical relation in long-channel MOSFET. 6

 b. Explain the charge sharing phenomenon in dynamic circuits. 6

 c. Explain the parameters which have impact on circuit limits while designing for low power circuits. 8

UNIT - II

3 a. Obtain the signal flow graph for direct and transpoled direct form of FIR system. 8

 b. Analyze the power optimization using operation reduction maintaining throughout. 4

 c. Discuss the technology mapping by considering area and power. 8

4 a. Obtain the data flow graph of IIR filter. 4

 b. Analyze the parallel and pipelined implementation along with diagram and expression. 8

 c. Obtain the algorithm for power dissipation driven multilevel logic optimization. 8

UNIT - III

5 a. Analyze the power consumption in a CMOS circuit defined by $y = \overline{(x_1 + x_2) x_3}$. 4

 b. Obtain the leakage summary in deep sub micrometer transistors. 8

 c. Compare the performance of single gate and dual gate SOI MOSFET along with schematic. 8

6 a. Analyze the performance of general structure of DCVS logic. 6

 b. Draw the schematic of short channel transistor, showing the various components of leakage currents. 8

 c. Discuss the surface potentials of short and long channel division. 6

UNIT - IV

7 a. With graphical approach, analyze the principles of sub threshold reduction. 6

 b. Compare the performance of conventional CMOS dynamic inverter with that of ADL CMOS inverter. 6

c.	Obtain the clock waveforms along with the interconnected 4 ADL inverters	8
8 a.	Realize the schematic of 2 input NAND gate using MTCMOS concept and inverter using DTMOS concept.	10
b.	Analyze the performance of 2N-2N2D inverters/buffer schematic.	6
c.	Obtain the schematic of 2 inputs ADL NAND gate.	4

UNIT - V

9 a.	Briefly analyze the services of software power dissipation.	12
b.	Discuss the access graph for code fragment and hence analyze partitioned access graph.	8
10 a.	Briefly explain the algorithm transformation to match computational resources.	10
b.	Discuss with necessary arrangements, the sample memory and register allocation constraints.	10

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