U.S.N | | | | | | | | | | |

P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Third Semester, B.E. – Electronics and Communication Engineering

Semester End Examination; Dec - 2016/Jan - 2017

Digital Electronic Circuits

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a. Explain with a neat circuit diagram, the working of two input basic (NAND) TTL gate. 8

b. With the help of circuit diagram, explain the working of two input NMOS NAND gate and two input PMOS NOR gate. 7

c. Define the following terms: 5

i) Power dissipation ii) Propagation delay.

2 a. Explain with the circuit diagram, the operation of ECL NOR gate. 10

b. Explain the operation of n-channel depletion type MOSFET with neat diagram and V-I characteristics. 10

UNIT - II

3 a. Obtain the complement of the following function : 5

$f(w,x,y,z) = \bar{w}x\bar{z} + w(x + \bar{y}z)$.

b. Obtain the minimized Boolean Expression for the following, 10

i) $f(w,x,y,z) = \sum m(0,1,2,3,4,9,13) + \sum \phi(5,10,11,14)$

ii) $f(w,x,y,z) = \pi m(0,3,4,11,13) + \pi\phi(2,6,8,9,10)$.

c. Design a three input and one output combinational logic circuit that has logic '1' output when the majority of inputs are at logic '1'. 5

4 a. Simplify using QM minimization technique, 12

$f(v,w,x,y,z) = \sum m(4,5,9,11,12,14,15,27,30) + \phi(1,17,25,26,31)$.

b. Simplify the following function using MEV technique, 8

$f(a,b,c,d) = \sum M(2,3,4,5,13,15) + \sum \phi(8,9,10,11)$.

Use 2 variable VEM and 3 variable VEM.

UNIT - III

5 a. Realize the following Boolean expression using 3 to 8 line decoder and OR gates, 6

$f_1(x,y,z) = \sum m(1,2,4,5)$

$f_2(x,y,z) = \sum m(1,5,7)$

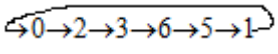
Contd.....2

	b.	Design a 4 to 2 line priority encoder.	8
	c.	Realize: $f(w,x,y,z)=\sum m(0,1,5,6,7,9,12,15)$ using multiplexer.	6
6	a.	Design and implement the following functions using PLA, $f_1=\sum m(0,1,3,4); \quad f_2=\sum m(1,2,3,4,5).$	10
	b.	Design a 2-bit magnitude comparator.	10

UNIT - IV

7	a.	Explain Gated SR Latch with diagram.	8
	b.	Explain the function and working of Gated D latch.	8
	c.	Explain how SR latch can be used as switch?	4
8	a.	Explain the working of master-slave JK flip-flop.	10
	b.	Explain the working of master-slave SR flip-flop.	10

UNIT - V

9	a.	Explain the working of a universal shift register with a neat circuit diagram.	10
	b.	Design a synchronous Mod-6 up counter using clocked JK flip-flop for the count sequence  and repeat.	10
10	a.	Explain with a neat diagram the architecture of 86 processor.	10
	b.	Explain the structure of PSW register of 86.	6
	c.	What do you mean by memory segmentation?	4

* * *