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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Third Semester, B.E. - Electrical and Electronics Engineering

Semester End Examination; Dec - 2016/Jan - 2017

Digital Electronics

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a. What are the different levels of Integration? 6

b. Prove that : 6

i) $AB + A(B+C) + B(B+C) = B + AC$ ii) $A\bar{B}C + \bar{A}BC + ABC = A(B+C)$.

c. Simplify the following Boolean Expressions : 8

i) $(\bar{A}+C)(\bar{A}+\bar{C})(\bar{A}+B+\bar{C}D)$

ii) $\bar{X}\ Y\ +\ X\ Y\ +\ X\ \bar{Z}\ +\ X\ \bar{Y}\ \bar{Z}$.

2 a. State and prove distributive law and redundant literal rule. 6

b. Find the complements of following given Boolean expression : 6

i) $\bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + +A\bar{B}\bar{C} + AB\bar{C}$

ii) $\bar{A}\ B + A\overline{BC} + \bar{A}\ B\ C\ D + \bar{A}\ \overline{BC}\ \bar{D}\ E$.

c. Implement the basic gates using universal gates. 8

UNIT - II

3 a. Differentiate between a prime implicant and a non-prime implicant and an essential prime implicant and a non-essential prime implicant with an example. 8

b. What is full adder? Realize using NAND gates. 6

c. Reduce using mapping the expression and implement using AOI logic 6
F = Σm (2, 3, 6, 7, 8, 10, 11, 13, 14).

4 a. What is parallel adder? Design Four bit look ahead carry generator. 10

b. Obtain the minimal sum of products for the function, 10
F(A, B, C, D) = Σm(1, 2, 3, 5, 6, 7, 8, 9, 12, 13, 15) using Quine Mc-Clusky method.

UNIT - III

5 a. Give the comparison between multiplexer and demultiplexer. 5

b. With the help of logic diagram and truth table explain D flip-flop and S-R flip-flop. 10

c. Design Octal to Binary Encoder. 5

Contd.....2

6	a.	Give comparison between decoder and encoder.	4
	b.	What is race around condition in flip-flop? Explain how it is eliminated?	8
	c.	Design BCD to decimal decoder with the use of decoder.	8

UNIT - IV

7	a.	Explain Mealy and Moore models of a clocked synchronous sequential network.	8
	b.	Design of a synchronous Mod-6 counter using J-K Flip-Flops.	12
8	a.	With neat timing diagram, explain 4-bit SISO's and PISO register.	12
	b.	With the help of logic diagram and state diagram, explain the operation of johnson counter and ring counter.	8

UNIT - V

9	a.	With the help of a neat diagram, explain the working of successive-approximation type ADC.	10
	b.	With the help of a neat diagram, explain the operation of a 2-input CMOS NOR gate.	10
10	a.	With the help of a neat diagram, explain the working R-2R ladder network type DAC.	12
	b.	With neat circuit diagram, explain the operation of a 2-input NAND gate with Totem pole output.	8

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