



P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belgaum)

Third Semester, B.E. - Information Science and Engineering

Semester End Examination; Dec - 2016/Jan - 2017

Digital Design

Time: 3 hrs

Max. Marks: 100

Note: Answer **FIVE** full questions, selecting **ONE** full question from each unit.

UNIT - I

- 1a. Explain with examples :
- i) Principle of duality ii) De-Morgan's law. 10
- iii) Minterm canonical form iv) Sequential network.
- b. Find essential prime implicants using QM technique of the following expression, 10
- $$f(w, x, y, z) = \sum m(7, 9, 12, 13, 14, 15) + dc(4, 11).$$
- 2 a. What are universal gates? Justify the same. 10
- b. Consider a four input A, B, C and D circuit and one output 'Z'. Output 'Z' is high, if input 'B' or input 'C' is high, but not both, else the output is zero. Design a minimum hardware circuit using K-map. 10

UNIT - II

- 3 a. Mention the building blocks of arithmetic circuits. Explain each of them with circuit diagram. 10
- b. Implement the following using 4 : 1 MUX and 8 : 1 MUX, 10
- $$f(w, x, y, z) = \sum m(0, 1, 5, 6, 7, 8, 9, 10, 15).$$
- 4 a. What is a magnitude comparator? Explain 1-bit and 2-bit magnitude comparator giving relevant equations. 10
- b. Design a 5-bit odd parity generator. 5
- c. Implement the following expressions using 3 : 8 decoder, 5
- $$f(A, B, C) = \sum m(0, 2, 4, 6)$$
- $$f(A, B, C) = \sum m(1, 3, 5, 7)$$
- $$f(A, B, C) = \sum m(0, 3, 4, 7).$$

UNIT - III

- 5 a. Differentiate between PLA and PAL. Realize the following expressions using PAL and PLA, 10
- $$f(A, B, C) = \sum m(1, 2, 4, 5, 7)$$
- $$f(A, B, C) = \sum m(0, 3, 6, 5, 7)$$
- $$f(A, B, C) = \sum m(0, 1, 4, 5, 7).$$
- b. Write VHDL code to implement full adder. 5

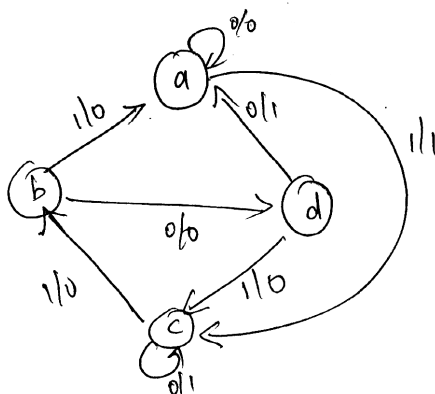
- c. What is binary ladder? Explain with an example. 5
- 6 a. Implement the following using PROM, 5
 - $f(A, B, C) = \sum m(1, 2, 3, 5, 7)$
 - $f(A, B, C) = \sum m(0, 2, 3, 4, 6)$
 - $f(A, B, C) = \sum m(1, 4, 6)$.
- b. Write VHDL/Verilog code to implement 4 : 1 MUX using bus representation. 5
- c. With a neat block diagram and circuit diagram, explain 4-bit D/A converter. 10

UNIT - IV

- 7 a. Explain 4-bit SIPO shift register giving the circuit diagram, truth table and wave diagram. 10
- b. Give characteristic equation, state diagram and excitation table of JK flip flop. 5
- c. Convert D flip flop to JK flip flop. Give state synthesis table and circuit diagram. 5
- 8 a. Briefly explain the different applications of shift register. 10
- b. Explain edge triggered JK flip flop. 5
- c. Convert T flip flop to SR flip flop. 5

UNIT - V

- 9 a. Design a mod 8 counter using T-flip flops. 10
- b. Mention and explain the various issues with asynchronous sequential circuits with examples. 10
- 10 a. Briefly explain 3-bit ripple counter giving its circuit diagram and truth table. 5
- b. Construct a Mealy model that detects a sequence 10110. 5
- c. A sequential network has one input and one output. The state diagram is as shown below. Design a sequential circuit using T flip flop. 10



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