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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Eighth Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; May/June - 2018

ASIC Design

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a. What are the sequences of steps used to design an ASIC? Draw the flow diagram for the ASIC design. Also, comment on logical and physical design. 12

b. Analyze the advantages and disadvantages with the use of FPGA and full custom ASIC. 8

2 a. Explain how Carry Save Adder (CSA) reduces carry rippling in addition. How are 4-bit CSA constructed using 3-bit CSA? What is the need for inserting latches in the 4-bit CSA? 8

b. What does each ASIC cell contain when ASIC cell libraries are designed? Explain each of them in detail. 10

c. Define ASIC and give two example for non-ASIC and ASICs. 2

UNIT - II

3 a. Analyze the working of three-state bidirectional output buffer. A device has 33 input/output (I/O) cells each drawing 30 mA while switching. If all the I/O cells switch simultaneously, what will be the power-supply bounce, if current changes from 0 to 1 A in 5 ns and power-supply inductance are 2 nH? 8

b. Recode the unsigned Binary number B = 00010111 as CSD vector D. 5

c. Consider 2X drive NOR3 logic cell in C_5 technology with each input driven with a 1X inverter, compute the delay. Given logic ratio r = 1.5 and C_{out} = 0.3 pF. 7

4 a. Determine the optimum path delay for the logic cascade chain shown in Fig. Q 4(a). Also, compute the input capacitance C2, C3 and C4. Ignore *p* and *q* of each stage. Assume logical ratio, r = 2, C1 = 1 pF. 10

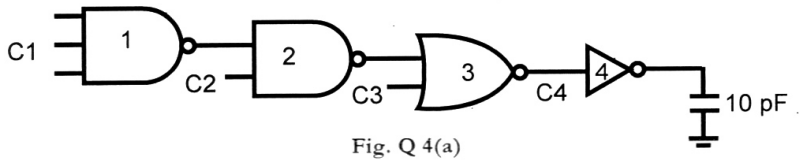

Fig. Q 4(a)

b. For a cascaded chain of N inverters each with equal stage effort, compute the value of stage electrical effort for minimum delay. 5

c. For a CMOS AOI221 logic cell shown in Fig. Q 4(c), compute logical effort and logical area for logic ratio, r = 2 5

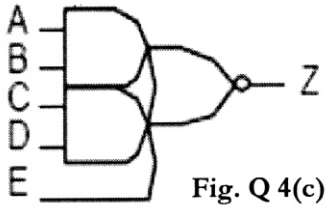

Fig. Q 4(c)

Contd...2

UNIT - III

5a. What is the need for hierarchical design? With suitable example, explain the hierarchical design. Also, explain how to label the nets in the hierarchical design. 10

b. What is netlist screener? List the errors that can be found by it. 5

c. What is logic synthesis? What are ways of optimization performed during logic synthesis? Explain them. 5

6a. Explain the basic structure of CFI 1.0.0 base connectivity model. 8

b. Analyze various types of simulation performed in ASIC design flow. 6

c. What is EDIF? Write the hierarchical nature of an EDIF file and explain. 6

UNIT - IV

7a. What is the need of methods and algorithms in CAD tool designing? Discuss the types of algorithms/functions used to reduce complexity. 8

b. Mention the steps used in constructive partitioning algorithm. 6

c. An ASIC chip has 40000 Flips-flops with input capacitance of clock input to each Flip-flop is 0.025 pF with clock frequency of 200 MHz, chip size of 20 mm on a side and clock spine consists of 200 lines across the chip with interconnect capacitance of 2 pF/cm and V_{dd} of 3.3 V, calculate; 6

i) Number of stages to drive the clock spine

ii) Power dissipated while charging the input capacitance of Flip-flop

iii) Power dissipated while driving clock spine iv) Peak current if rise time is 0.1 ns

8a. What are the various iterative placement improvement algorithms used to improve the existing placement solutions? Explain with examples to each. 10

b. What is slicing in floor-planning? Illustrate with an example. What are cyclic constraints? How do you resolve them? 7

c. Why the stem of a T-junction has to be routed first? Explain with example. 3

UNIT - V

9a. What is the sequence of steps used in timing-driven floor planning and placement design (physical design flow)? With the help of flow diagram explain each step. 10

b. Find the global channel density for the channel shown in Fig. Q 9(b). 2

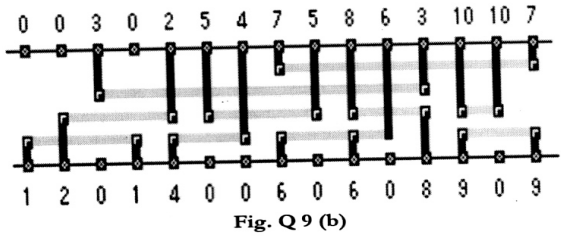

Fig. Q 9 (b)

c. Explain global routing between the blocks and inside the flexible blocks. 8

10a. Illustrate with an example Lee-maze-running algorithm. 5

b. Demonstrate the left-edge algorithm with an example. List all the steps. 8

c. What is circuit extraction? Illustrate the various formats in which the parasitic information is passed back. 7

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