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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Sixth Semester, B.E. - Computer Science and Engineering

Semester End Examination; May/June - 2018

Computer Architecture

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a. Describe grain sizes and latency in program partitioning and scheduling. 8

b. Explain Flynn's classification of computer architecture with neat diagrams. 7

c. Briefly explain the five generations of electronic computers. 5

2 a. List and explain different data dependencies among instructions and also write the dependence graph for the following instructions :

Load R_1, A

Add R_2, R_1

Move R_1, R_3

Store B, R_1 8

b. With a neat diagram, explain any two models of shared memory multiprocessors. 8

c. With a block diagram, explain generic model of a message passing multicomputer. 4

UNIT - II

3 a. With a neat diagram, explain architectural distinction between CISC and RISC machines. 4

b. Give four differences between superscalar and VLIW processor. 6

c. Briefly explain two methods of interleaved memory organization. 4

d. Define bus arbitration with suitable sketch. Explain centralized bus arbitration method. 6

4 a. Explain VLIW processor with VLIW instruction format and pipelined execution of VLIW instructions with diagrams. 10

b. Define instruction pipelines. Explain the pipeline execution in a base scalar processor and also explain two cases in which under pipelined executor occurs. 10

UNIT - III

5 a. Explain two types of pipeline models with neat diagram. 8

b. Briefly explain the Arithmetic pipeline design. 6

c. Explain prefetch buffers and hazard avoidance mechanisms for instruction pipelining to improve pipeline throughput. 6

6 a. With respect to linear pipeline processor, explain : 10

i) Asynchronous and synchronous models ii) Speedup, efficiency and throughput

Contd…2

b.	Briefly explain the methods of static and dynamic branch handling strategies.	6
c.	Define dynamic pipeline .Explain how pipeline frequency in determined?	4

UNIT - IV

7 a.	What do you mean by cache coherence problem? Explain directory based protocols to handle coherence problem.	10
b.	Explain the concept of deadlock in virtual channels.	10
8 a.	Explain snoopy based protocols.	8
b.	With neat diagram, explain store-forward and worm hole routing scheme of message passing.	8
c.	Explain how test and reset and set instructions can be used to enforce synchronization?	4

UNIT - V

9 a.	Explain the steps involved in developing a parallel application.	8
b.	With a block diagram, explain shared address space protocol in scaling process.	8
c.	Write a note on simulation of ocean currents with respect to parallel applications.	4
10 a.	Explain the goals of parallelization.	8
b.	What is scalability? Explain bandwidth and latency scaling.	8
c.	Explain synchronous message passing protocol.	4

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