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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Sixth Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; May/June - 2018

Digital Design Using Verilog HDL

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1	a.	Illustrate the different system tasks and compiler directives with examples.	10
	b.	Develop the verilog description and stimulus for 4:1 multiplexer using gate level modeling.	10
2	a.	Develop the verilog description and stimulus for 4-bit ripple carry full adder.	8
	b.	Write the verilog code for 4 to 1 multiplexer using conditional operators.	6
	c.	Develop a verilog code for T flip-flop in dataflow description.	6

UNIT - II

3	a.	Explain the following with an example : i) Always statement ii) Event based timing control iii) Conditional statements	10
	b.	Develop a verilog module to generate a bit-wise nor of two *n*-bit buses.	10
4	a.	Explain the different loop statements with example.	10
	b.	Explain function declaration and invocation with example.	10

UNIT - III

5	a.	Develop verilog code for D flip-flop with procedural continuous assignments.	10
	b.	Explain different types of delay models with example.	6
	c.	Explains MOS switches.	4
6	a.	Develop the switch level verilog model stimulus for two inputs NOR gate.	10
	b.	Briefly discuss the flow diagram of delay back Annotation.	10

UNIT - IV

7	a.	Develop a verilog model and stimulus for 4-to-1 multiplexer with UDP.	10
	b.	Explain simulation flow using PLI routines.	10
8	a.	Develop a verilog UDP description for negatively edge triggered D flip-flop with clear.	10
	b.	Explain basic computer-aided logic synthesis process.	10

UNIT - V

9	a.	Develop a verilog model for newspaper vending machine FSM.	10
	b.	Explain the process of traditional verifications flow with the help of flow chart.	10
10	a.	Explain Architectural modeling.	6
	b.	Briefly discuss the verifications methodology with a hardware accelerator.	8
	c.	Briefly explain assertion checking.	6

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