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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Sixth Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; May / June - 2018

VLSI Testing and Verification

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each Unit.*

UNIT - I

1 a. Briefly discuss the VLSI technology trends affecting testing as increase in transistor density. 8

b. Explain digital and analog VLSI testing in digital circuits. 8

c. Explain the role of testing in VLSI. 4

2 a. Explain Boolean difference for test generation techniques for combinational circuits. Also realize the Boolean difference of $F = X_1X_2 + X_3X_4$ with respect to X_4. 6

b. Explain PODEM algorithm for test generation combinational circuits. 8

c. Explain transistor stuck ON and stuck open faults in CMOS. 6

UNIT - II

3 a. Illustrate the Reed-Muller expansion technique. 8

b. Illustrate the synthesis of random pattern testable combinational circuits. 6

c. Design testable PLA for following Boolean function : 6

i) $Z_1 = XY + X\bar{Y}$, $Z_2 = \bar{X}Y$ using PLA

ii) $F_1 = \bar{W}X + W\bar{X}Y + \bar{W}\bar{X}Y$, $F_2 = WX\bar{Y} + W\bar{X}Y$, $F_3 = \bar{W}\bar{X}Y + W\bar{X}Y + WX\bar{Y}$

using Fujiwara's approach.

4 a. Illustrate test generation based on functional fault models. 10

b. Explain state table verification along with example. 10

UNIT - III

5 a. Illustrate scan-path technique for testable sequential circuit design. 10

b. Explain architecture of boundary scan. 10

6 a. Explain the following with respect to output response analysis : 10

i) Transition ii) Syndrome checking iii) Signature analysis

b. Along with logic diagram and BIST architecture, design BILBO and STUMPS. 10

UNIT - IV

7 a. Discuss the cycle based and event based simulation with suitable examples. 10

b. List out limitations of linting tools. 10

8. Write a short note on: 20

i) Code coverage ii) Waveform viewers iii) Functional coverage iv) Assertions

Contd…2

UNIT - V

9	a.	Illustrate verification strategies in verification plan.	10
	b.	Briefly explain the coverage-Driven Random-Based approach in verification plan.	10
10	a.	Illustrate various levels of verification plan.	10
	b.	Briefly explain about role of verification plan.	10

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