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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Sixth Semester, B.E. - Electrical and Electronics Engineering

Semester End Examination; May/June - 2018

Embedded Systems

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a. i) Derive the equation for percentage revenue loss for any market rise angle θ. 4

ii) A product was delayed by 5 weeks in releasing to market. The peak revenue for the product for on time entry to market would occur after 10 weeks. If a company whose product entered the market on time earned a total revenue of $ 25 million, how much revenue did the company that entered the market 5 months late case? 6

b. With an example explain the different classifications of an embedded system. 10

2 a. Define the three main IC technologies. What are the benefits of using each of the three different IC technologies? 10

b. What are the characteristics of an embedded system design? List and briefly explain the design metrics used to compare them. 10

UNIT - II

3 a. Explain the various events that take place when a processor executes an instruction. How pipelining improves the execution speed? 10

b. Briefly explain the purpose of the data path and controller in a single purpose processor. 10

4 a. Explain how a stepper motor is controlled using driver. Give relevant hardware and software details. 10

b. Given an analog input signal whose voltage ranges from 0 to 5 V, and an 8-bit digital encoding. Calculate the correct encoding for 3.5 V and then trace the successive approximation approach to find the corect encoding. 6

c. Explain how watch-dog timer is used in ATM? 4

UNIT - III

5 a. What is memory hierarchy? How does the cache operate? Discuss the direct cache mapping technique. 10

b. With a neat diagram, explain the advanced RAM architecture. 6

c. Sketch the internal design of a 4 x 3 ROM. 4

6 a. Explain port and bus-based I/o addressing of microprocessor interfacing. 10

b. Describe the I^2C and IEEE 802.11 protocols. 10

Contd…2

UNIT - IV

7	a.	Explain the fundamental issues in hardware software co-design.	10
	b.	Explain the significance of Data Flow Graph (DFG) and Control Data Flow Graph (CDFG) in embedded system.	10
8	a.	What are the building blocks of UML? Explain in detail.	10
	b.	Explain the important hardware software 'trade-offs' in hardware software partitioning?	5
	c.	Design an automatic tea/coffee vending machine based on; i) Initiated by user inserting a 5 rupee coin ii) The user can select coffee / Tea or cancel the order Draw Fson model for the system.	5

UNIT - V

9	a.	Describe shared data problem with an example. Show how disable / enable interrupt can be used for sloving this problem?	10
	b.	Mention the factor that effects interrupt latency.	4
	c.	What are the three different states of task in RTOS? How is the state of each task tracked?	6
10	a.	With an example, illustrate the problems of 'Delay embrace' and 'Priority inversion'.	10
	b.	With example, explain Round-Robin architecture. What are its limitations? How do you overcome the limitations of Round-Robin architecture?	10

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