



P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Second Semester, M.Tech - Computer Engineering (MCEN)

Semester End Examination; May/June - 2018

ARM Based Processor

Time: 3 hrs

Max. Marks: 100

Note: Answer FIVE full questions, selecting ONE full question from each unit.

UNIT - I

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|---|----|--|----|
| 1 | a. | Explain how instruction set is designed with example? | 10 |
| | b. | Briefly explain pipelining. Discuss its Hazards and efficiency. | 10 |
| 2 | a. | Discuss the features of RISC machines that are used and rejected in ARM processor. | 10 |
| | b. | Explain the following features of ARM programmer's model : | 10 |
| | | i) CPSR ii) memory system iii) ARM instruction set | |

UNIT - II

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|---|----|---|----|
| 3 | a. | Write an ARM assembly language program to print r_1 content in hexadecimal. | 8 |
| | b. | Explain the shift and rotate instructions of ARM with example. | 12 |
| 4 | a. | With a neat diagram explain 5-stage pipeline organization. | 10 |
| | b. | Explain ARM high speed multiplier organization with a diagram. | 10 |

UNIT - III

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|---|----|---|----|
| 5 | a. | Explain the following instructions : | 10 |
| | | i) SWP ii) BL iii) SWI iv) TST | |
| | b. | Explain co-processor data operations and data transfers with Binary encoding. | 10 |
| 6 | a. | Explain the ARM floating point architecture. | 14 |
| | b. | Explain the standard ARM C program address space model. | 6 |

UNIT - IV

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|---|----|--|----|
| 7 | a. | Explain Thumb instruction decomposer organization and Thumb ARM instruction mapping. | 14 |
| | b. | Explain the Thumb branch instructions with Binary coding and example (any three). | 6 |
| 8 | a. | Explain in detail Advanced Microcontroller Bus Architecture (AMBA). | 16 |
| | b. | Explain any two Debug approaches of ARM. | 4 |

UNIT - V

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|----|----|--|----|
| 9 | a. | With a neat diagram, explain direct mapped cache organization. | 10 |
| | b. | Explain the organization of ARM7 TDMI and ARM-8. | 10 |
| 10 | a. | Explain Two-Way set Associative cache with a neat diagram. | 10 |
| | b. | Explain any Ten CPIS MMU Registers. | 10 |