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# P.E.S. College of Engineering, Mandya - 571 401

***(An Autonomous Institution affiliated to VTU, Belagavi)***

**Second Semester, M. Tech - VLSI Design and Embedded System (MECE)**

**Semester End Examination; May/June - 2018**

**Design of Analog and Mixed Mode VLSI Circuits**

*Time: 3 hrs* *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

**UNIT - I**

1a. Starting from fundamentals derive the expression for drain current $I_D$ for MOS transistor. Also obtain the expressions for, i) $I_{D(max)}$ ii) $I_D$ in triode version iii) $R_{on}$. Sketch the V-I characteristics. 10

b. Derive the small signal model of MOS transistor. Obtain the expression for $G_m$, $r_o$ and $G_{mb}$. Also sketch the complete model with capacitances included. 10

2a. Derive the expression for voltage gain of CS stage when it is driving,
i) Diode connected load ii) Current source load 10

b. Obtain the expression for voltage gain of CG stage driving the load $R_D$ and driven by a voltage source of internal resistance $R_S$. The effects of channel length modulation and body effect must be considered. 10

**UNIT - II**

3 a. For a basic differential pair show that the small-signal differential gain is given by,
$|A_v| = R_D \left\{ \sqrt{M_n C_{ox} \frac{W}{L} I_{ss} R_D} \right\}$ 10

b. i) Write a note on Gilbert cell ii) Illustrate how current mirror processes the signal? 10

4 a. Discuss the common mode response of a differential pair. How the common mode response gets affected due to i) Resistor mismatch ii) Finite tail capacitance. 10

b. Discuss the large signal and small signal analysis of active current mirror. 10

**UNIT - III**

5 a. Discuss Gain boosting and output impedance boosting in differential cascode stage. 10

b. Discuss the response of linear Op-Amp to step input. 10

6 a. Discuss the effect of Op-Amp offset on the reference voltage. Explain how it is reduced? 10

b. Write explanatory note on the following :
i) PTAT current generation ii) Constant – $G_m$ biasing. 10

**UNIT - IV**

7 a. Sketch and explain the time response of unity gain samples in amplification mode. Derive the expressions for $\frac{V_o(S)}{V_1(S)}$ and Zamp starting from its equivalent circuit. 10

Contd…2

b. Write explanatory note on the following : 10

i) Channel charge injection ii) Clock feed through iii) $K_T/C$ noise

8 a. Develop the linear model of 3 stage ring oscillator and i) obtain $\frac{V_o(S)}{V_1(S)}$

ii) Find and plot the poles for different gain conditions 10

iii) Obtain the expression for $V_o(t)$

b. For a colpitts oscillator obtain the expression for i) $\frac{V_{out}}{I_{in}}$

ii) Frequency of oscillations 10

iii) Minimum gain for sustained oscillations

**UNIT - V**

9 a. For a type-I PLL

i) Sketch the linear model

ii) Obtain the open and closed loop transfer functions 10

iii) Find the expressions for $W_n$, G and poles

iv) Obtain the step response assuming under damped systems.

b. Explain the operation of simple charge pump PLL and develop its linear model deriving transfer function of each block. Also obtain open and closed loop transfer functions. 10

10 a. Write an explanatory note on :

i) Jitter in PLLS 10

ii) Delay locked loop

b. Discuss the following applications of PLL :

i) Skew reduction 10

ii) Jitter reduction

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