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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Second Semester, M. Tech - VLSI Design and Embedded System (MECE)

Semester End Examination; May/June - 2018

Low Power VLSI Design

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a.	Explain the static and dynamic power dissipation in CMOS circuits.	8
b.	Briefly discuss voltage, physical capacitance and activity factor in the power optimization process.	8
c.	Mention the four principal in low power.	4
2 a.	Briefly explain the following in VLSI Design : i) Dynamic dissipation in CMOS ii) Transistor sizing and optimal gate oxide thickness	10
b.	Discuss the impact of technology scaling and innovation trends for low power devices.	10

UNIT - II

3 a.	Mention the types of Adders. With neat diagram, explain Ripple Carry Adder.	10
b.	Describing the working of the current mode adders.	10
4 a.	Explain the principal of Multiplier. Mention its advantage and disadvantage.	6
b.	With neat diagram, explain 8-bit Wallace Tree Multiplier.	8
c.	Draw the neat diagram of 4 x 4 unsigned Braun Tree Multiplier.	6

UNIT - III

5 a.	Explain the source of power dissipation in DRAM.	10
b.	Discuss low power SRAM circuit techniques.	10
6 a.	Explain state and dynamic flip-flops with example.	10
b.	In detail, explain the importance of CMOS low power cell library for digital design.	10

UNIT - IV

7 a.	Discuss the new materials for wires and dielectrics.	10
b.	Discuss the following in low power VLSI design : i) Interconnection delay ii) Crosstalk	10
8 a.	Briefly explain power and performance management in low power systems.	10
b.	Write short notes on : i) Guarded Evaluation ii) Glitch Reduction by Pipeling.	10

UNIT - V

9 a.	Discuss the design techniques for safety critical application.	10
b.	Write a note on low power subsystem design.	10
10 a.	Explain the single driver versus distributed buffers.	10
b.	With the help of relevant block diagram, explain the chip and package code design of clock network.	10

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