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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Second Semester, M. Tech - VLSI Design and Embedded System (MECE)

Semester End Examination; May/June - 2018

ARM Processor

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1a.	With a block schematic, explain bus interface and memory system of ARM Cortex M3.	10
b.	Discuss the applications of ARM Cortex-M processors.	5
c.	What is Thumb-2 technology? Mention it's importance in ARM Cortex M processor	5
2a.	Explain the advantages of Cortex – M processors.	10
b.	Mention the important features need to be considered while designing a product using Cortex- M microcontrollers.	6
c.	How ARM Cortex – M3 processor is compatible with other ARM devices.	4

UNIT - II

3.a.	With a neat sketch explain the bit fields of floating point status and control register.	10
b.	Discuss the role of stack memory in Cortex – M processors	6
c.	Write a short note on Fault handling.	4
4 a.	With an example explain aligned ad unaligned data transfer in little endian memory system. Mention the limitations of Cortex – M processors to support unaligned data transfer.	10
b.	Explain the features of Nested vectored interrupt controller (NVIC) in Cortex – M processors.	10

UNIT - III

5 a.	Discuss the importance of special registers used for interrupt making and also write core – function for masking in interrupts.	10
b.	Discuss tail chaning and pop preemption exception behaviors of as applicable to interrupt handling.	10
6 a.	Explain in detail how cortex – M processors uses stacking when an interrupt occurs.	10
b.	List and describe system exceptions interrupts used in Cortex – M3 or Cortex – M4	10

UNIT – IV

7 a.	With a neat diagram explain how an interrupt is detected by the Cortex – M processor in the absence of clock signals.	10
b.	Explain the low power characteristics of the Cortex – M processors.	4
c.	With a neat flow chart explain WFE for task synchronization in a multiple core system.	6

Contd…2

8 a.	Discuss the features of sub- region Disable(SRD)	10
b.	Compare MPU (Memory Protection Unit) features between Cortex – Mo+ and Cortex – M_3/M_4 processor.	5
c.	Briefly explain the functionality of MPU type registers.	5

UNIT - V

9.a	Explain fault exception handlers in Cortex – M processors.	10
b.	Discuss stack trace, event trace and instruction trace in analysing faults.	10
10 a.	Explain debug operation modes in Cortex – M processors.	10
b.	Discuss Instrumentation trace macro cell (ITM) in Cortex – M processors.	10

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