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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Second Semester, M. Tech - VLSI Design and Embedded System (MECE)

Semester End Examination; May/June - 2018

Design of VLSI System

Time: 3 hrs

Max. Marks: 100

Note: Answer FIVE full questions, selecting ONE full question from each unit.

UNIT - I

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| 1 a. Explain in detail of structured design techniques. | 10 |
| b. Explain the terms: | |
| i) Programmable logic devices | 10 |
| ii) Programmable inter connect | |
| 2 a. Explain the concept of hierarchy in VLSI design. | 5 |
| b. Write a short note on full custom design. | 5 |
| c. Briefly explain the EDA tools for system. | 10 |

UNIT - II

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| 3 a. Explain the following design capture tools: | |
| i) HDL design | 10 |
| ii) Schematic design | |
| b. Discuss different types of simulation tools used in verification of VLSI system. | 10 |
| 4 a. With necessary arrangements, explain the chip composition high-lighting the progression of steps at each level. | 5 |
| b. Explain the terms: | |
| i) Time Verifiers | 15 |
| ii) Network isomorphism | |
| iii) Netlist comparision | |

UNIT - III

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|---|----|
| 5 a. Draw the schematic diagram of a comparator to compare the magnitude of two 4-bit binary number using adders. Explain the operation for unsigned and signed comparison. | 10 |
| b. Design a 16-bit carry select adder using 4-bit adder, in each group write expression for critical path delay. | 10 |
| 6 a. With an example show how the multiplication is performed using radix-4 booth encoding. Explain in brief. | 10 |
| b. Draw the basic ROM architecture using programmable ROM and NAND ROM and explain its working. | 10 |

UNIT - IV

- 7 a. Explain the FSM design procedure with an example. 10
- b. Discuss the power distribution employed while designing special purpose subsystem. 10
- 8 a. Explain the global clocking strategies in modern VLSI design of PLL. 10
- b. With a neat diagram, explain the working of CMOS inverter as an amplifier. 10

UNIT - V

- 9 a. Explain in detail about fault models. 5
- b. Explain how serial and parallel scan testing is implemented. 5
- c. Explain the terms :
- i) Recurring cost 10
- ii) Non-curring cost
- 10 a. Explain in brief, boundary scan techniques. 10
- b. Discuss different types of fault models in VLSI design. 10

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