U.S.N | | | | | | | | | | |

P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Second Semester, M. Tech - VLSI Design and Embedded System (MECE)

Semester End Examination; May/June - 2018

Advanced in VLSI Design

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a. Compare and contrast Bi-CMOS and CMOS technology. 6

b. Draw the transfer plot of CMOS inverter and hence describe role of aspect ratio of *n*-channel and *P*-channel MOSFET'S in CMOS inverter with suitable mathematical analysis. 8

c. Derive an expression for drain current in saturation and Non-saturation region of nMOS transistor. 6

2a. Draw typical MESFET structure. Explain its working and obtain an expression for; 12

i) Drain current below pinch off voltage ii) Pinch off voltage

b. How is modulation doping achieved in the construction of a HEMT device? Explain with a diagram the MODFET structure and contrast the MODFET with a MESFET. 8

UNIT - II

3 a. Using the energy band diagram of MIS diode, explain the meaning of V_T. 8

b. What are the basic properties of ideal MJS system? Briefly explain them. 8

c. An *n*-channel MIS device has the following parameters : 4

$N_A = 10^{17}/cm^3$, $Q_i = 10^{11}$ q/cm^2, d = 20 nm and φ_{ms} = -0.95 V.

Calculate the threshold voltage V_T for the device.

4 a. Explain processing challenges to further CMOS miniaturization. 10

b. What are the effect of short channel on the performance of MOSFET device? Explain the concept of channel length modulation. Plot variation of the threshold voltage with the channel length. 10

UNIT - III

5 a. What are the advantages of molecular materials? Briefly explain. 8

b. Compare and contrast the scaling rules for the all three cases : 6

Constant field, Constant voltage and Quasi-constant voltage

c. Compare and contrast bulk MOSFET and SOI MOSFET devices and show that the bulk device is more susceptible to short-channel effects than the SOI device is. 6

Contd…2

6 a. What is defect tolerant computing? Compare and contrast Family tree structure and Fat-tree architecture. 8

b. Explain the principle and working of a molecular diode with molecular structures. Explain equilibrium, forward and reverse bias condition with energy level diagram. 8

c. Sketch SOI MOSFET structure and briefly explain how the device performance is better compared to conventional MOSFETs? 4

UNIT – IV

7 a. What is a super buffer? What is the main advantage of a super buffer? With neat diagrams explain inverting and non-inverting type nMOS super buffers. 10

b. In the arrangement of Fig. 7(b), the load capacitance is large; develop a scaled chain of N inverters such that the delay time between the logic gate and the load capacitance node is minimized. 10

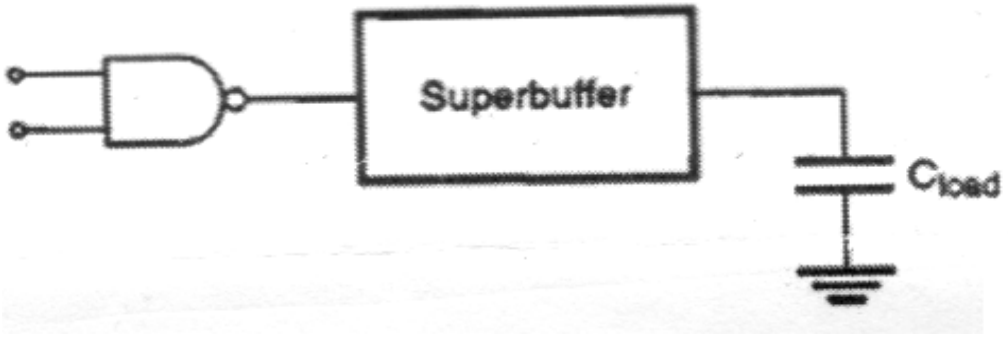

Fig. 7(b)

8 a. Show that when an RC delay line is long, the signal delay tend to infinity and suggest means to improve the performance of the delay line. 10

b. Implement the function,

$$Y = \overline{(A + B + C).D}$$ 10

Using CMOS gates and draw the stick diagram for the same.

UNIT - V

9 a. Draw the arrangement for a 1 x 4 multiplexer using nMOS switches, develop its stick diagram and mask layout. Briefly explain. 8

b. Draw the circuit of a 4 x 4 barrel shifter, develop its stick diagram and standard cell 2-mask layout. Briefly explain. 12

10 a. What is cell-based design? What are its advantages? Develop a typical standard cell layout (with constraint) and briefly explain. 10

b. With suitable example explain the following terms : 10

i) Locality ii) Regularity

iii) Hierarchy iv) Modularity

* * * *