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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Sixth Semester, B.E. - Computer Science and Engineering

Semester End Examination; May/June - 2019

Advance Computer Architecture

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a. Illustrate layered development of parallel computers based on the classification by Lionel Ni. 8

b. What is MIPS rate? A workstation uses a 1.5 GHz processor with a claimed 1000 MIPS rating to execute a given program mix. Assume a one cycle delay for each memory access what is the effective CPI of this computer? 4

c. Define the following terms for various system interconnect architectures :

i) Node degree ii) Network diameter iii) Bisection bandwidth

Find the same for the following Network type :

I) RING II) STAR III) MESH (completely connected) 8

2 a. List shared memory multiprocessor. Explain any two with neat diagram. 8

b. The program consists of 4 major types of instruction. The instruction mix and number of cycle (CPI) needed for each instruction type is given below. Calculate the average CPI when the program is executed on a uni-processor? 4

	Instruction Type	CPI	Instruction Count
1	Arithmetic and logic	1	60%
2	Load / store with cache hit	2	18%
3	Branch	4	12%
4	Memory reference with cache miss	8	10%

c. List data dependence types. 2

d. Construct 8×8 Omega Network. 6

UNIT - II

3 a. Compare the instruction set architecture in RISC and CISC processors in terms of instruction formats addressing modes, CPI and CPU control. 8

b. Demonstrate time sequence of information transfer between a master and a slave over a system bus. 7

c. Define Memory swapping. Distinguish between Non-preemptive allocation and Preemptive allocation scheme. 5

Contd…2

4 a. Explain architecture of a Very Long Instruction Word (VLIW) processor and its pipeline operation. 10

b. Construct backplane buses, system interface and slot connections of various functional boards in multiprocessor system and explain briefly. 10

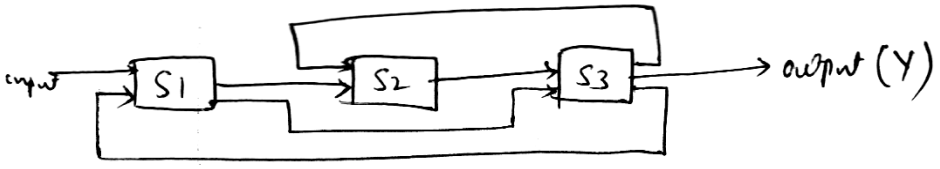
UNIT - III

5 a. Explain two models of linear pipeline units and the corresponding reservation table. 10

b. Show the representation of 32 bit floating point number using IEEE754 floating point standard. Find the sign bit, exponent and mantissa for the binary number $1.10011001100110011001100 \times 2^{-4}$ 10

6 a. Define pipelining. List and explain the various types of pipeline hazards. 7

b. Find the reservation table, initial collision vector, forbidden latencies and state diagram for the following three stage pipeline.



9

c. Explain Tomasul'o dynamic instruction scheduling. 4

UNIT - IV

7 a. List three major characteristics of an inter connection network, construct 2 stage 64×64 butterfly switch network of 8×8 cross bar switches. 8

b. Discus write invalidate and write update policies for maintaining cache consistency. 8

c. Explain wormhole routing scheme of multicomputer system. 4

8 a. Distinguish between blocking and non-blocking networks. List cross bar limitation. 5

b. Discuss three types of cache directory protocols with neat diagram. 9

c. Explain any two flow control methods for resolving a collision between two packets requesting the same outgoing channel. 6

UNIT - V

9 a. Explain pseudocode describing the orchestration of data parallel equation solve problem under shared address space. 10

b. List issues to be considered in a primitive network transaciton. Explain any ten. 10

10 a. Explain Dancehall multiprocessor organizaiton . 5

b. List and explain the steps in the parallelization processes. 6

c. Define scalability. Explain the following : 9

i) Bandwidth scaling ii) Latency scaling

iii) Cost scaling iv) Physical scaling

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