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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Sixth Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; May/ June - 2019

Digital Design Using Verilog HDL

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a. Describe the different types of system tasks with examples. 8

b. Develop a verilog model and stimulus of 8:1 multiplexer using conditional operator. 6

c. Explain the sized and un-sized numbers with examples. 6

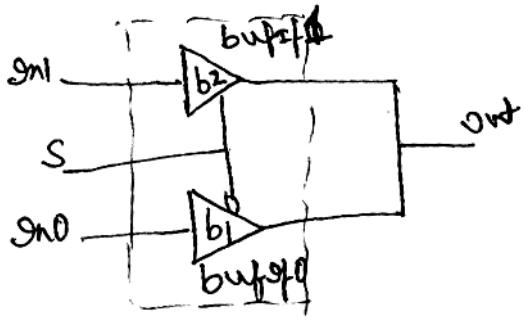
2 a. Design and develop a verilog mode and stimulus of 6 bit parallel adder using gate level description. 8

b. Design a 2-to-1 multiplexer using bufif 0 and bufif 1 gates.

The delay specification for gates b1 and b2 are as follows:

	Min	Typ	Max
Rise	1	2	3
Fall	3	4	5
Turn off	5	6	7

Apply stimulus and test the output values. 6



c. Mention the different delays in data flow modeling and explain them with examples. 6

UNIT - II

3 a. Describe the event based timing control mechanism using behavioral modeling with examples. 8

b. Explain the sequential and parallel blocks with examples. 6

c. Develop a verilog model of a 8:3 priority encoder using case z-statement. 6

4 a. Develop a verilog model of a 4:16 decoder using conditional statement. 6

b. Describe the difference between tasks and functions. 6

c. Design and develop a verilog model of eight function ALU that takes two four bit numbers *a* and *b*, computes a five bit result based on a three bit select signal using function. 8

Contd…2

UNIT - III

5	a.	Explain the different types of delay models with examples.	6
	b.	Define system tasks for timing checks and explain with examples.	8
	c.	Design and develop the verilog model of a 4-to-1 multiplexer using transmission gates (switch level).	6
6	a.	Discuss the flow diagram of delay back annotation.	6
	b.	Explain the usage of keywords assign and de assign using an example.	8
	c.	Develop the switch level model of a 3 input CMOS nand gate.	6

UNIT - IV

7	a.	List the User Defined Primitives (UDP) rules of verilog language.	8
	b.	Mention the guidelines for User Defined Primitive (UDP) design explain.	6
	c.	Explain how PLI routine is used in a verilog simulation.	6
8	a.	Mention the types of design partitioning in logic synthesis and briefly explain with examples.	6
	b.	Explain the logic synthesis flow from Register Transfer Level (RTL) to gate level netlist.	8
	c.	Write the uses of Programming Language Interface (PLI).	6

UNIT - V

9	a.	Develop a verilog model for RTL description for news paper vending manchine FSM.	10
	b.	Explain the functional verification flow environment.	10
10	a.	Explain with block diagram formal verification and equivalence checking.	10
	b.	Briefly discuss the flow chart of traditional verification flow.	10

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