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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Sixth Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; May / June - 2019

VLSI Testing and Verification

Time: 3 hrs *Max. Marks: 100*

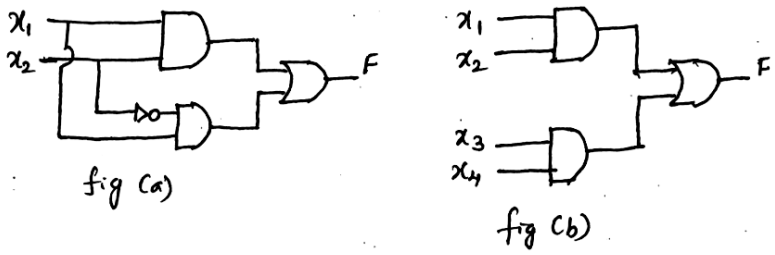
***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a. Differentiate between testing and verification. Briefly discuss the VLSI technology trends affecting testing as increase in transistor density. 10

b. Define fault. Briefly discuss fault models in use today with examples. 10

2 a. Consider the logic circuits shown in Fig. (a) and Fig. (b). Find the Boolean difference with respect to x_2 and x_3 respectively. 10



b. Explain PODEM algorithm function with neat block diagram. 10

UNIT - II

3 a. Explain Reed-Muller expansion technique for direct implementation. 10

b. With a neat diagram, explain different testable PLA design approaches. 10

4 a. Explain test generation based on functional fault models using state table with example and also list the steps involved in state encoding process. 10

b. Explain homming tree sequence for machine *M* and *N* with state table and example. 10

UNIT - III

5 a. Explain controllability and observability with a neat block diagram. 6

b. Explain how the ADHOC design rules are used for improving testability with examples? 8

c. Explain LSSD design rules. 6

6 a. List the classification of test pattern generation for BIST scheme and explain Pseudo-exhaustive LFSR / SR test pattern. 10

b. Explain the BILBO architecture with the help of neat block diagram. 10

UNIT - IV

7 a. Explain linting tools with example. 5

b. Discuss the cycle based and event based simulation with suitable example. 10

c. Write a short note on verification IP. 5

Contd…2

8	a.	Write a short note on code coverage.	6
	b.	Discuss the verification languages and issues tracking in verification tools.	8
	c.	Briefly explain code related and quality related metrics.	6

UNIT - V

9	a.	Illustrate the various levels of verification plan.	10
	b.	Explain the verification strategies.	10
10	a.	Illustrate the directed test benches approaches in verification plan.	10
	b.	Explain the coverage driven random-based approach in verification plan.	10

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