U.S.N ☐ ☐ ☐ ☐ ☐ ☐ ☐ ☐ ☐ ☐

P.E.S. College of Engineering, Mandya - 571 401
(An Autonomous Institution affiliated to VTU, Belagavi)
Eighth Semester, B.E. - Electronics and Communication Engineering
Semester End Examination; May / June - 2019
Algorithm for VLSI Physical Design Automation

Time: 3 hrs   *Max. Marks: 100*

*Note: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

|		
1 a.	Briefly outline the steps of VLSI design cycle.	12
b.	Discuss the full custom design style.	8
2 a.	Explain any five specific fabrication processes in detail.	10
b.	Discuss the design rules for the circuit layout.	10

UNIT - II

3 a.	List the different issues related to the fabrication process and explain any three in detail.	12
b.	Explain the advances in Lithography and Interconnects.	8
4 a.	With an example, explain the different graph search algorithm.	8
b.	Explain the various operations performed on a layout using the corner stitch data structure.	12

UNIT - III

5 a.	Explain the parameters considered during the partitioning at different design styles.	10
b.	Explain simulated evoluation algorithm in detail.	10
6 a.	List out different classification of floor-planning algorithm. Explain Integer Programming Based floor-planning.	10
b.	Explain channel pin assignment.	10

UNIT - IV

7 a.	With the help of flowchart, explain the two-phase routing.	10
b.	Draw all net types and routings patterns for routing graph in Fig. 7(a)	10

fig. 7(a)
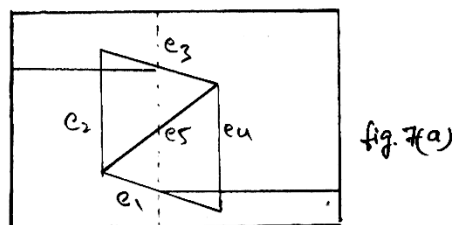
8 a.	With the help of neat diagram, explain scanline algorithm.	12
b.	Explain Constraint Graph Based Hierarchical compaction.	8

UNIT - V

9 a.	Discuss about the calculation of delay for buffered and un-buffered clock trees.	10
b.	Explain exact Zero skew algorithm.	10
10 a.	Explain the routing network models.	10
b.	Explain the routing algorithm for non-segmented model.	10

* * * *