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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Fourth Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; May / June - 2019

Digital Design Using Verilog HDL

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1	a.	What is meant by stopping and finishing in a simulation? Explain with an example.	6
	b.	Write verilog descriptions for 4-bit ripple carry full adder by making use of 1-bit full adder.	8
	c.	Write verilog description (data flow) of 4:1 multiplexer.	6
2	a.	Obtain the design hierarchy for SR latch simulation.	6
	b.	Write a verilog description for module D given by, $y = (ab + c)$ with gate delay AND = 4 and OR = 5.	6
	c.	Obtain verilog description (data flow) for edge-triggered D flip flop.	8

UNIT - II

3	a.	Write a verilog description (behavioral) of 4:1 MUX.	8
	b.	Using wait statement, design a level sensitive latch with clock d as Input and $q = d$ when clock = 1.	6
	c.	Obtain verilog code for parity calculator using 'Function' with 32-bit address.	6
4	a.	Write a verilog description for 4-bit counter (behavioral).	6
	b.	Design 4 to 1 MUX using if and else statements.	6
	c.	Write a verilog code (using 'Function') for 32- bit left / right shifter.	8

UNIT - III

5	a.	Analyze the use of VCD file in the debug process with neat block diagram.	8
	b.	Define setup and hold time. Explain with an example.	6
	c.	Obtain the switch level verilog descriptions of 2 to 1 MUX.	6
6	a.	Design a positive edge triggered D flip flop with asynchronous clear and present using assign statement.	6
	b.	Explain delay back annotation with the help of flow diagram.	8
	c.	Obtain the switch level verilog code for CMOS flip flop.	6

UNIT - IV

7	a.	Design a negative edge-triggered JK flip flop with asynchronous preset and clear as a UDP.	6
	b.	Obtain the general process of adding and invoking a user defined system task.	6
	c.	What are the limitations of logic synthesis?	8

Contd…2

8	a.	Design a level sensitive D latch with preset, input *d* clock and output *q*.	6
	b.	Discuss the role of access and utility routines with block diagram.	6
	c.	Analyze the basic computer Aided logic synthesis process.	8

UNIT - V

9	a.	Interpret verilog constructs and translate it to logic gates.	8
	b.	Explain the various components in traditional verification flow.	12
10	a.	Obtain the finite state machine for news paper vending machine.	12
	b.	Explain the various components of a functional verification environment.	8

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