U.S.N | | | | | | | | | | |

P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Second Semester, M. Tech - VLSI Design and Embedded System (MECE)

Semester End Examination; May / June - 2019

Low Power VLSI Design

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1	a.	Explain the basic principles of low power design.	4
	b.	Briefly outline the needs for low power VLSI design.	6
	c.	Explain the different sources of power dissipation on CMOS circuits.	10
2	a.	Discuss the impact of technology scaling and innovation trends for low power devices.	10
	b.	Briefly explain the following in VLSI design : i) Dynamic dissipation CMOS ii) Transistor sizing and Gate oxide	10

UNIT - II

3	a.	Discuss in detail the architecture of CMOS adder.	10
	b.	What are the current mode adders? Describe the working of current mode adders in detail.	10
4	a.	With a neat diagram, explain the working of Braun tree multiplier.	10
	b.	Write a note on 8-bit Wallace Tree Multiplier.	10

UNIT - III

5	a.	Discuss low power SRAM circuit techniques.	10
	b.	Explain the sources of power dissipation in SRAM and DRAM.	10
6	a.	Write a note on high capacitance node.	10
	b.	Discuss in detail the working of dynamic flip flops.	10

UNIT - IV

7	a.	Discuss in detail new materials used for wires and dielectrics.	10
	b.	Discuss the following in low power VLSI design : i) Inter connection delay ii) Cross talk	10
8	a.	Explain the parallel architecture with voltage reduction.	10
	b.	Discuss the power and performance management of low power architecture.	10

UNIT - V

9	a.	Write a note on low power subsystem design.	10
	b.	Discuss the design techniques for safety critical applications.	10
10	a.	With the help of relevant block diagram, explain chip and package co-design of clock network.	10
	b.	Explain Zero skew versus Tolerable skew.	10

* * * *