U.S.N | | | | | | | | | | |

P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Second Semester, M. Tech - VLSI Design and Embedded System (MECE)

Semester End Examination; May/June - 2019

ARM Processor

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1	a.	Explain how Cortex-M4 processor is different from Cortex-M3 processor.	8
	b.	Explain compatibility nature of Cortex-M processor with other ARM devices.	7
	c.	List the advantages of Cortex-M processors.	5
2	a.	With a neat block diagram, explain various bus interfaces on the Cortex-M3 and Cortex-M4 processor.	10
	b.	Briefly explain OS support and system level features of Cortex-M processor.	10

UNIT - II

3	a.	List and explain memory system features of Cortex-M processors.	10
	b.	Mention the significance of stack memory and also explain the instructions used to access the stack memory.	10
4	a.	Explain memory access attributor of Cortex-M3 and Cortex-M4 processor.	10
	b.	Discuss the importance of memory system feature which leads to more flexible memory map arrangement.	10

UNIT - III

5	a.	List and explain different exception types of interrupts.	10
	b.	With necessary block diagram, explain relocation feature of vector table in Cortex-M processors.	10
6	a.	What is interrupt masking? With an example, explain how special register are used for interrupt masking?	10
	b.	Explain the SCB registers for Application Interrupt and Reset Control Register (AIRCR).	10

UNIT - IV

7	a.	With necessary diagram, explain sleep-on-exit feature of Cortex-M processor.	10
	b.	What is low power design? Mention its benefits and also explain low power system requirements of Cortex-M processors.	10
8	a.	With a neat diagram, explain different ways to divide an MPU using sub-region durable feature for efficient memory utilization.	10
	b.	With associated flow chart, explain the stepwise process of setting up of memory protection unit.	10

Contd…2

UNIT - V

9	a.	Illustrate, how system handler control and state register (SCB > SHSCR) are used to enable fault exceptions?	10
	b.	List and explain various techniques / tools used for analyzing faults in Cortex-M processors.	10
10	a.	Explain debug modes in Cortex-M processors.	10
	b.	Compare advantages of ETM trace with MTB trace.	6
	c.	List the types of trace source in Cortex-M processors.	4

* * * *