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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Second Semester, M. Tech - VLSI Design and Embedded System (MECE)
Semester End Examination; May/June - 2019
Design of Analog and Mixed Mode VLSI Circuits

Time: 3 hrs Max. Marks: 100

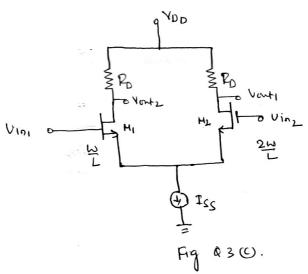
Note: Answer FIVE full questions, selecting ONE full question from each unit.

UNIT - I

- 1 a. Discuss the following second order effects in MOS device:
 - i) Body effect ii) Ch
- ii) Channel length modulation
 - b. For a common source stage using diode connected load, obtain the expression for voltage gain using small signal model.
 - c. For a source follows obtain the expression for A_{ν} .
- 2 a. For a common gate stage, obtain the expression for voltage gain taking channel length modulation into consideration.
- b. Derive the expression for output impedance of cascade stage.
- c. Compare common source and common gate amplifier with respect to voltage gain, input impedance and output impedance.

UNIT - II

- 3 a. For a differential amplifier with current source load, obtain the expression for voltage gain. Suggest a method to increase the voltage gain.
 - b. Explain the operation of Gilbert cell.
 - c. For the circuit of Fig. 3(c), calculate the small signal gain given that, width of M_1 is one half of that of M_2 and bias values of V_{in1} and V_{in2} are equal.



4 a. What is a current mirror? What are its applications? Explain the operations of cascade current mirror.

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b.	For a differential amplifier with current mirror, obtain the expression for common mode	10				
	gain A _{CM} .	10				
	UNIT - III					
5 a.	Discuss the implementation of two stage Op-Amp. Explain how gain boosting is done?	10				
b.	What is the need for common mode feedback? Discuss how common mode feedback is					
	done using resistive sensing and source followers?	10				
6 a.	What is a band gap reference? Discuss the generation of temperature independent voltage.	8				
b.	Discuss the generation of PTAT.					
c.	What is the need for constant G_m biasing? Explain how constant G_m biasing is done using	6				
	switched capacitor resistor?	6				
	UNIT - IV					
7 a.	Discuss the response of sampling circuit to differential input levels with initial conditions.	6				
b.	Discuss the following effects in switched capacitor circuits:					
	i) Channel charge injection	8				
	ii) Clock feed through					
c.	Explain the operation of unity gain sample in sampling mode and amplification mode.	6				
8 a.	For Colpitts oscillator derive the expression for:					
	i) Condition for sustained oscillators	10				
	ii) Frequency of oscillators					
b.	What is V_{C0} ? Explain the important performance parameters of V_{C0} .	10				
	UNIT - V					
9 a.	Develop the linear model of type-I PLL and obtain its step response.	10				
b.	A cellular telephone incorporates a 900 MHz PLL to generate the carry frequencies.					
	If $W_{LPF} = 40 \pi kHz$ and the output frequency is to be changed from 901 MHz to 901.2 MHz,	4				
	how long does the PLL output frequency take to settle with in 100 Hz of its final value?					
c.	Discuss how the addition of frequency detection increases the acquisition range?	6				
10 a.	What is delay locked loop? Explain its construction.	10				

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b. Explain how PLL can be used to eliminate skew?