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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Third Semester, B.E. - Computer Science and Engineering

Semester End Examination; Dec. - 2019

Digital Logic Design

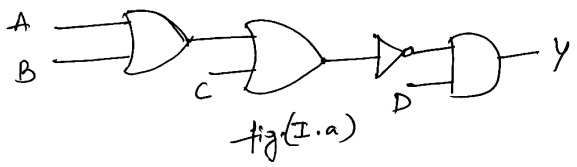
Time: 3 hrs *Max. Marks: 100*

Course Outcomes

The Students will be able to:

CO1 - Design simplified logic circuits using Boolean equation minimization techniques.
CO2 - Design the data processing circuits.
CO3 - Design memory circuits.
CO4 - Design shift registers and counters using flip-flops.
CO5 - Derive state machine models for sequential circuits and write VHDL code for all logic circuits.

Note: I) **PART - A** is compulsory. One question for 2 marks from each unit.
II) **PART - B**: Answer any **two** sub questions (from a, b, c) for Maximum of 18 marks from each unit.

Q. No.	Questions	Marks
	I : PART - A	**10**
I a.	Get the output for the following circuit shown in fig (I.a.)  fig (I.a)	2
b.	Define parity generator and checker.	2
c.	Write the truth table for SR flip-flop.	2
d.	List types of registers.	2
e.	Write VHDL code for 1:4 Multiplexer.	2
	II : PART - B	**90**
	UNIT - I	**18**
1 a.	i) Define Universal gate. Realize basic gates using NOR gate. ii) Simplify the following Boolean expression : $f(A,B,C) = ABC + A\bar{B}C + AB\bar{C} + A$	9
b.	Simplify the following Boolean function using k-map : *i)* $f(p,q,r) = \Pi M(0,2,4,6) + d(1,3)$ *ii)* $f(a,b,c,d) = \sum m(1,3,7,11,15) + d(0,2,4)$ *iii)* $f(a,b,c,d) = \sum m(2,4,6,12,13) + d(0,3,15)$	9
c.	Using Quine McCluskey method, solve the following Boolean function, $F(a,b,c,d) = \sum m(0,3,4,5,7,10,14,15)$	9

Contd...2

UNIT - II **18**

2 a. Implement $U = ad + b\bar{c} + bd$ using: i) 16:1 MUX ii) 8:1 MUX. 12

b. i) Implement the following using 3:8 decoder:

$f_1(w, x, y, z) = \sum m(0, 1, 3, 4)$ and $f_2(w, x, y) = \sum m(2, 4, 6, 7)$ 12

ii) Design full adder using two half adders.

c. Design 3-bit binary to grey code converter using basic gates. 6

UNIT - III **18**

3 a. Implement the following Boolean function using PAL and PLA :

i) $f_1(a, b, c) = \sum m(0, 1, 2, 3, 7)$

ii) $f_2(a, b, c) = \sum m(3, 5, 6, 7)$

iii) $f_3(a, b, c) = \sum m(1, 2, 6, 7)$ 9

b. Convert SR flip flop to JK flip-flop. 9

c. Define race around conditions. Explain JK Master slave flip-flop with neat logic diagram. 9

UNIT - IV **18**

4 a. Explain Ring counter and Johnson counter with example and logic diagram. 9

b. Design mod-6 Synchronous Up counter using D flip flop. 9

c. Design mod-8 Asynchronous counter using JK flip flop. 9

UNIT - V **18**

5 a. Give the ASM chart for vending machine problem and explain the same. 12

b. Write VHDL code for the following logic circuits:

i) 4:2 Encoder

ii) D flip-flop

iii) Full subtractor 12

c. Differentiate between Moore model and Mealy model. 6

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