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## P.E.S. College of Engineering, Mandya - 571401

(An Autonomous Institution affiliated to VTU, Belagavi)
Third Semester, B.E. - Computer Science and Engineering Semester End Examination; Dec. - 2019

Computer Organization
Time: 3 hrs
Max. Marks: 100
Note: i) PART - A is compulsory. Two marks for each question.
ii) PART - B: Answer any Two sub questions (from $a, b, c$ ) for Maximum of 18 marks from each unit.

| Q. No. | Questions | Marks |
| :---: | :---: | :---: |
|  | I : PART - A | $\mathbf{1 0}$ |

I a. Write a neat diagram of processor cache. 2
b. Give input/output instructions. 2
c. List the steps involved in execution of a complete instruction. 2
d. Give the memory hierarchy of a computer. 2
e. Write generate and propagate function of carry lookahead addition. 2

II : PART - B 90
UNIT - I 18
1 a. Describe basic functional units of a computer with a neat diagram. 9
b. Explain the connection between the processor and the memory in detail. 9
c. i) Brief explains Big-Endian and Little-Endian methods. 9
ii) Write basic performance equation and briefly explain the parameters.

UNIT - II
2 a. List and explain the various addressing modes with an example. 14
b. Write an ALP to add $N$ numbers stored in memory and store the result in memory. 14
c. Explain the instruction associated with substances call and return. 4

UNIT - III 18
3 a. With a block diagram, explain single bus organization of the data path inside a processor. 14
b. Explain the execution of the instruction Add (R3), R1. 14
c. Explain memory mapped I/O and programmed controlled I/O. 4

UNIT - IV 18
4 a. Explain with diagram the organization of ROM. 9
b. Explain different mapping techniques of cache memory with a diagram. 9
c. Explain memory performance consideration. 9

UNIT - V 18
5 a. Explain 4 bit carry Lookahead adder. 9
b. Explain hardware arrangement for sequential circuit binary multiplier with block diagram. 9
c. Explain IEEE standard for floating point numbers with example each. 9

