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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

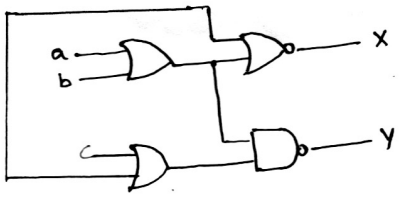
Third Semester, B.E. – Computer Science and Engineering

Semester End Examination; Dec. - 2019

Digital Logic Design

Time: 3 hrs *Max. Marks: 100*

Note: I) **PART - A** is compulsory. One question for 2 marks from each unit.
II) **PART - B**: Answer any **two** sub questions (from a, b, c) for Maximum of 18 marks from each unit.

Q. No.		Questions	Marks
		I : PART - A	**10**
I	a.	State duality principle with example.	2
	b.	Explain de-multiplexer with the help of block diagram.	2
	c.	Give any two differences between sequential and combinational circuit.	2
	d.	List: i) Types of register ii) Application of shift register.	2
	e.	Give verilog structural code for the following Fig.QI(e):  Figure Q1(e)	2
		II : PART - B	**90**
		UNIT - I	**18**
1	a.	Give the truth table for the following function and reduce the same using k-map technique. $F(A,B,C,D) = \Pi M(0,3,4,7,8,10,12,14) + d(2,6)$	6
	b.	Define min term, max term, negative logic and positive logic. Simplify the following function using k-map technique and implement using Basic gates $F(A,B,C,D) = \overline{A}\,\overline{B}D + AB\overline{C}\,\overline{D} + \overline{A}BD + ABC\overline{D}$	12
	c.	Simplify the following expression using tabulation method and give the circuit for essential prime implicant. $F(A,B,C,D) = \sum m(1,3,6,7,8,9,10,12,14,15) + d(11,13)$	12
		UNIT - II	**18**
2	a.	What is magnitude comparator? Design one bit comparator using basic gates.	9

Contd…2

b. Explain 4-line to 16-line decoder with relevant circuit shows a 3 to 8 decoder and multi-input OR gates, following Boolean expressions can be realized simultaneously,

$F_1(A,B,C) = \sum m(0, 2, 6)$
$F_2(A,B,C) = \sum m(1, 2, 3, 7)$
$F_3(A,B,C) = \sum m(4, 7)$ 9

c. Explain multiplexer in detail. Implement the following function using 8:1 multiplexer:

$F(A,B,C,D) = \sum m(0,2,4,5,8,11,14) + d(1,7,15)$ 9

UNIT - III **18**

3 a. Convert the following flip flop and draw the circuit:

i) SR flip flop to JK flip flop ii) SR flip flop to T flip flop 9

b. Give the state transition, characteristic equation, and excitation table for SR, JK and D flip flop. 9

c. With a neat circuit diagram explain Programmable Logic Array (PLA). Design 7-segment decoder using PLA. 9

UNIT - IV **18**

4 a. With a relevant circuit, wave form and truth table explain ripple down counter. 9

b. Explain the following:

i) Switched tail Counter
ii) Sequence Generator and Sequence Detector
iii) Serial Adder 9

c. Design a mod-5 synchronous counter using JK flip flop and implement the same. 9

UNIT - V **18**

5 a. Give the output function transition table and state diagram by analyzing the sequential circuit shown in Fig. (a).

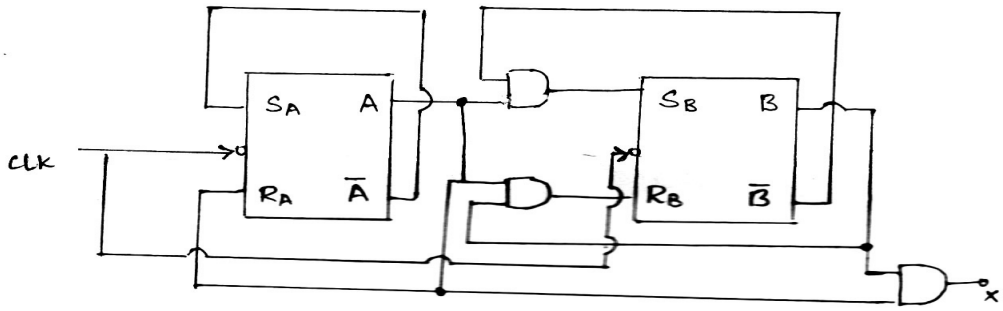


figure Q5(a) 12

b. Give the state synthesis table, design equation and circuit diagram for vending machine problem (Mealy Model). 12

c. Write the VHDL code for :

i) D-flip flop ii) 8:1 Multiplexer 6

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