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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Third Semester, B.E. - Computer Science and Engineering

Semester End Examination; Dec. - 2019

Computer Organization

Time: 3 hrs *Max. Marks: 100*

Note: **i) PART - A** is compulsory. **Two** marks for each question.
ii) PART - B: Answer any **Two** sub questions (from a, b, c) for Maximum of **18 marks** from each unit.

Q. No.	Questions	Marks
	I : PART - A	**10**
I a.	Write the basic performance equation of a computer and explain its parameters.	2
b.	Define word and word length of a computer memory.	2
c.	Mention the operations performed by a branch instruction.	2
d.	List and explain I/O interface registers used in the data transfer operations.	2
e.	Compare static RAM and dynamic RAM.	2
	II : PART -B	**90**
	UNIT - I	**18**
1 a.	List the steps needed to execute the machine instruction Add LOCA, R_0 in terms of transfers between processor and memory.	9
b.	With a block diagram, explain different functional units of a computer.	9
c.	Explain the following terms: i) Pipelining and Super scalar operation ii) CISC and RISC iii) Multiprocessor and Multicomputer	9
	UNIT - II	**18**
2 a.	Explain different addressing modes and give examples for each.	9
b.	Which are the different ways of word assignments? Explain the same. Consider a computer that has a byte addressable memory organized in 32-bit words. A program reads characters "COMPUTER" entered at a keyboard and stores them in successive byte locations. Show the contents of the memory words in different word assignments.	9
c.	Write an assembly language program for adding *n* numbers.	9
	UNIT - III	**18**
3 a.	Explain the concept of stack frames in subroutines.	9
b.	Write an assembly language program to evaluate the following: $A = B + C * D + E$. Assume no carry and borrow.	9
c.	Briefly discuss how I/O tasks are performed in a program controlled I/O.	9

Contd…2

UNIT - IV **18**

4 a. With a neat diagram, explain the single bus organization of the data path inside a processor. 9

b. Mention an interrupt mechanism which addresses simultaneous arrivals of interrupt requests from two or more devices. Further explain the same and mention its one advantage. 9

c. State any two advantages of Direct Memory Access. With a neat diagram, explain the arbitrations scheme where single device participate in the selection of bus master. 9

UNIT - V **18**

5 a. Explain any one cache mapping functions. A block set associative cache consists of a total of 64 blocks divided into 4 block sets. The main memory contains 4096 blocks, each consisting of 128 words, 9

i) How many bits are there in a main memory address?

ii) How many bits are there in each of the TAG, SET and WORD fields?

b. Explain IEEE standard representations for floating point numbers. Further represent 3.24 in any one IEEE standard floating point formats. 9

c. Mention one advantage of Booth's algorithm. Multiply +23 * −10 using Booth's method and bit-pair recoding method. 9

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