U.S.N

P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Third Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; Dec. - 2019

Analog Electronic Circuits

Time: 3 hrs Max. Marks: 100

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a. Describe the operation of *n*-channel enhancement type MOSFET for the following voltage conditions: i) As V_{DS} is increased
ii) For $V_{DS} \geq V_{0V}$, write the drain current equation in both cases — 10

b. What is channel - length modulation? Derive the drain current equation in terms of 'λ' and write the large - signal equivalent circuit model of the *n*-channel MOSFET in saturation, incorporating the output resistance r_0. — 10

2 a. Consider a MOSFET process technology for which L_{min} = 0.4 μm, t_{ox} = 8 nm, μ_n= 450 cm^2/V.s, $\varepsilon_{ox} = 3.45 \times 10^{-11}$ and V_t = 0.7 V;
i) Find C_{ox} and k_n' — 10
ii) For a MOSFET with W/L = 8 μm/0.8 μm, calculate the value of V_{GS} and V_{DSmin} needed to operate the transistor in the saturation region with a dc current I_D = 100 μA

b. Why biasing is required in MOSFET amplifier with circuit diagram? Explain MOSFET biasing using a constant current source. — 10

UNIT - II

3 a. Describe the following:
i) Input and output offset voltages ii) Input bias current and input offset current — 10
iii) Offset Nulling

b. Draw the circuit diagram for an instrumentation amplifier. Analyze the circuit operation and show how the voltage gain can be varied? Also show that the common mode gain is one. — 10

4 a. Using a 741 Op-amp, design a capacitor-coupled non-inverting amplifier to have a voltage gain of 66. The input signal amplitude is 15 mV. The load resistor is 2.2 kΩ and the lower cutoff frequency is 120 Hz. — 10

b. Sketch the circuit of a high input impedance capacitor-coupled voltage follower. Analyze the circuit operation and also explain how to determine the capacitor values? — 10

UNIT - III

5 a. Show how feedback in an Op-amp inverting amplifier can produce instability? Define loop gain, loop phase shift, phase margin and explain the conditions necessary for oscillations to occur in an Op-amp circuit. — 10

b. Design the voltage sorce to provide an output of 9 V to a 500 Ω load. The available supply is ±12 V and the potentiometer is to be included to adjust for approximately ±10% tolerance on the Zener diode voltage . take I_Z = 20 mA and assume I_2 through R_2 and R_3 connected to emitter of transistor as 50 μA. 10

6 a. Design the inverting Schmitt trigger circuit to have UTP = 6 V and LTP = 3.5 V. Use a 741 Op-amp with V_{CC} = ±18 V. Draw the input and output voltage waveform for a triangular wave input. Use silicon diodes and assume voltage divider current as 100 μA. 10

b. Sketch the circuit for combination of two voltage level detectors to monitor a battery voltage (V_B) that gives one indication when the V_B is above threshold voltage and another indication when the supply is below a threshold voltage. Use LEDs for indication. Analyzes the circuit operation. 10

UNIT - IV

7 a. Show how a half-wave precision rectifier can be combined with a summing circuit to produce a full-wave precision rectifier? Draw the input and output voltage waveform write and explain the equations to show that full-wave rectification is performed. 10

b. Design an adjustable peak clipping circuit to clip at ±(3 to 5) V. The circuit is to have unity voltage gain.Assume 2 mA current through feedback resistor, and silicon zener diodes. 10

8 a. Sketch an Op-amp precision rectifier peak detector circuit, draw the input and output waveforms and explain the circuit operation. Write the equation for calculating the capacitor value for a peak detector circuit. 10

b. A ±5 V , 10 kHz square wave form a signal source with a resistance of 100 Ω is to have its positive peak clamped precisely at ground level. Tilt on the output is to be approximately 1% of the peak amplitude of the wave. Design a suitable precision clamping circuit. Use an Op-amp with a ±12 V supply 10

UNIT - V

9 a. Draw the circuit diagram of a triangular/rectangular waveform generator using Op-amps. Sketch the circuit wave forms and explain its circuit operation. 10

b. Design the RC phase shift oscillator circuit to produce a 3 kHz output frequency. The Op-amp is to use ±12 V supply . Assume A_{CL}= 29 and I_1 = 50 μA. 10

10 a. Sketch the cirucit of a series voltage regulator that uses an IC Op-amp as an error amplifier. Explain the circuit operation and write the equation for V_O in terms of V_Z. Briefly discuss the supply voltage requirement . 10

b. Desing an LM317 voltage regulator to provide 6 V output from a 15 V supply . The load current is 200 mA .Determine suitable resistance values for R_1 and R_2 and calculate the regulator power dissipation. Assume V_{ref} = 1.25 V. 10

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