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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Third Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; Dec. - 2019

Digital Electronic Circuits

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT -I

1 a. Explain the following parameters to characterize logic families:
i) Noise margin ii) Fan-out
iii) Power dissipation iv) Propagation delay — 8

b. Draw the circuit diagram and write the truth table of a two-input DTL NAND gate. — 6

c. Analyze the working of 2 input TTL totem pole NAND gate along with schematic. — 6

2 a. Explain the operation of n-channel enhancement type MOSFET with required diagram and I-V characteristics plot. — 8

b. Analyze the working of a two input NMOS nor gate with circuit diagram and truth table. — 6

c. Construct a 2-input CMOS NAND gate and explain its operation. — 6

UNIT - II

3 a. Simplify using k-map and determine SOP and POS expressions for the function,
$f(w, x, y, z) = \sum m(0, 1, 3, 7, 8, 12)+dc(5, 10, 13, 14)$. — 10

b. Given $f(w, x, y, z) = \sum m(1, 3, 4, 5, 6, 7, 11, 14, 15)$, using Karnaugh map,
i) Find the essential prime implicants
ii) Find the minimum sum of products
iii) Find all the prime implicants — 10

4 a. Simplify using QM minimization technique $f(w, x, y, z) = \sum m(0, 5, 6, 7, 9, 10, 13, 14, 15)$. — 10

b. Obtain a minimal sum for the incompletely specified Boolean function,
$f(w, x, y, z) = \sum m(0, 4, 5, 6, 13, 14, 15) + dc(2, 7, 8, 9)$ using VEM Map. — 10

UNIT - III

5 a. Describe the working of binary full adder and obtain the expression for sum and carry. Realize it using basic gates. — 8

b. Realize the following Boolean expressions,
$f_1(x_2, x_1, x_0) = \Pi M(0, 1, 3, 5)$ and $f_2(x_2, x_1, x_0) = \Pi M(1, 3, 6, 7)$ using 3:8 active low decoder with, i) OR gate ii) NOR gate. — 6

c. Design a 4-bit priority encoder assigning highest priority to the largest number. — 6

6 a. Implement the following Boolean function using, i) 8:1 mux ii) 4:1 mux
$f(x, y, z) = \sum m(0, 2, 3, 5)$. — 10

Contd…2

b. Design and implement the following expressions using $3 \times 4 \times 2$ PLA, 10

$f_1(x, y, z) = \sum m(0, 1, 3, 4)$ and $f_2(x, y, z) = \sum m(1, 2, 3, 4, 5)$

UNIT - IV

7 a. What is SR latch? Write its gate level logic diagram and function table. Illustrate its application as a switch de bouncer along with waveforms. 10

b. Describe with neat diagram the working of a master slave JK flip-flop using gated SR latch. 10

8 a. Explain the following with gate level schematic,

i) Gated SR latch 10

ii) Gated D latch

b. Analyze the working of positive edge triggered D-flip-flop with neat gate level schematic. 10

UNIT - V

9 a. Draw the logic schematic for the following shift registers,

i) SISO ii) SIPO iii) Universal shift register 10

Also write the mode control table for, iii) (Considering 3-bit registers)

b. Design a synchronous mod-6 counter for the following sequence, 10

0, 2, 3, 6, 5 using JK flip-flop.

10 a. Draw logic schematic for the following counters based on shift registers:

i) Mod-4 ring counter

ii) Mod-8 twisted ring counter 10

Also write the count sequence table for each.

b. Explain with a neat diagram the architecture of 8086 microprocessor. 10

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