



P.E.S. College of Engineering, Mandya - 571 401
 (An Autonomous Institution affiliated to VTU, Belagavi)
Fifth Semester, B.E. - Electronics and Communication Engineering
Semester End Examination; Dec - 2019
Digital CMOS VLSI Design

Time: 3 hrs

Max. Marks: 100

Note: Answer FIVE full questions, selecting ONE full question from each unit.

UNIT - I

- 1 a. With the help of relevant diagram, explain the structure and working of Metal Oxide Semiconductor (MOS). 6
- b. Develop the threshold voltage equation of a MOS transistor. 7
- c. Consider an n-channel MOS process with the following parameters:
 Substrate doping density $N_A = 10^{16} \text{ cm}^{-3}$, polysilicon gate doping density $N_D(\text{gate}) = 2 \times 10^{20} \text{ cm}^{-3}$, gate oxide thickness $t_{\text{ox}} = 50 \text{ nm}$ oxide interface fixed charge density $N_{\text{ox}} = 4 \times 10^{10} \text{ cm}^{-2}$ and source and drain diffusion doping density $N_D = 10^{17} \text{ cm}^{-3}$. In addition, the channel region is implemented with p-type impurities ($N_I = 2 \times 10^{11} \text{ cm}^{-2}$) to adjust the threshold voltage. The junction depth of the source and drain diffusion regions is $X_j = 1.0 \mu\text{m}$. Plot the variation of the zero-bias threshold voltage V_{TO} as a function of the channel length ($V_{\text{DS}} = V_{\text{SB}} = 0$) also find the V_{TO} for $\alpha = 0.7 \mu\text{m}$, $V_{\text{DS}} = 5 \text{ V}$ and $V_{\text{SB}} = 0$. 7
- 2 a. Explain the concept of constant field scaling. 6
- b. Analyze the short channel effects with relevant equations. 7
- c. Consider a simple abrupt pn-junction, which is reverse biased with a voltage V_{bias} . The doping density of the n-type region is $N_D = 10^{19} \text{ cm}^{-3}$, and doping density of the p-type region is given as $N_A = 10^{16} \text{ cm}^{-3}$. The junction area is $A = 20 \mu\text{m} \times 20 \mu\text{m}$. Calculate; 7
- i) C_{j0} ii) If input voltage changes from 0 to -5 V , calculate equivalent capacitance.

UNIT - II

- 3 a. Explain the depletion NMOS load inverter with relevant equation. 8
- b. Consider a CMOS inverter circuit with the following parameters:
 $V_{\text{DD}} = 3.3 \text{ V}$, $V_{\text{TO},n} = 0.6 \text{ V}$, $V_{\text{TO},p} = -0.7 \text{ V}$, $K_n = 200 \mu\text{A/V}^2$, $K_p = 80 \mu\text{A/V}^2$. Calculate the noise margin of the circuit ($K_R = 2.5$ and $V_{\text{TO},n} + |V_{\text{TO},p}|$). 12
- 4 a. Discuss the calculation of Interconnect delay of RC network. 8
- b. A company has access to a CMOS fabrication process with the device parameters listed below:
 $\mu_n C_{\text{ox}} = 120 \mu\text{A/V}^2$, $\mu_p C_{\text{ox}} = 60 \mu\text{A/V}^2$, $L = 0.6 \mu\text{m}$ for both nMOS and pMOS device, $V_{\text{TO},n} = 0.8 \text{ V}$, $V_{\text{TO},p} = -1.0 \text{ V}$, $W_{\text{min}} = 1.2 \mu\text{m}$. Design a CMOS inverter by determining the channel widths W_n and W_p of the NMOS and PMOS transistors, to meet the following performance specifications; 12

- i) $V_{th} = 1.5 \text{ V}$ for $V_{DD} = 3 \text{ V}$
- ii) $\tau_{PHL}^* \leq 0.2 \text{ ns}$ and $\tau_{PHL}^* \leq 0.15 \text{ ns}$
- iii) A falling delay of 0.35 ns for an output transition from 2 V to 0.5 V, assuming a combined output load capacitance of 300 fF and ideal step input.

UNIT - III

- 5 a. Analyze the CMOS NOR2 (Two-Input NOR) gate with relevant equations. 8
- b. Design the CMOS logic circuit for the function $Z = \overline{A(D+E)+BC}$. 5
- c. Analyze the bias conditions and operating regions of CMOS transmission gates. 7
- 6 a. With relevant diagrams and equations explain the behavior of Bistable elements. 8
- b. Design the CMOS SR latch circuits using NOR2 gates. 5
- c. Analyze the function of a CMOS implementation of the D-Latch. 7

UNIT - IV

- 7 a. Analyze the working principle of Pass transistor circuit for logic '1' transfer. 8
- b. Design and sketch the dynamic CMOS logic circuit for the Boolean function $Z = \overline{(A+B+C)+(BC)}$. 5
- c. Analyze the working principle of CMOS transmission gate dynamic shift register. 7
- 8 a. Design and sketch the Domino CMOS logic circuit for the Boolean function $Z = \overline{ABC+(B+C)}$. 5
- b. Analyze the working principle of True Single Phase Clock (TSPC) dynamic CMOS. 7
- c. Analyze the voltage boot strapping with relevant equations. 8

UNIT - V

- 9 a. Analyze the charge control model of BJTs with relevant diagram and equation. 10
- b. Discuss the switching delay in BiCMOS logic circuit with related circuits diagrams and waveforms. 10
- 10 a. Discuss the ESD protection adopted to protect the circuit with an example. 10
- b. Mention the guidelines for avoiding latch-up in CMOS circuit. 5
- c. Discuss the process of simple on chip clock generation using ring oscillator. 5

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