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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Seventh Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; Dec. - 2019

Analog CMOS VLSI Design

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a. Draw the small signal model of common source amplifier with source degeneration and derive an expression for the voltage gain and output resistance of the circuit. Assume $\lambda \neq 0, \gamma \neq 0$. 10

b. The circuit of Fig. 1.1 is designed to provide an output voltage swing of 2.2 V with a bias current of 1 mA and a small signal voltage gain of 100. Calculate the dimensions of M_1 and M_2. Assume $\mu_n C_{OX} = 1.3422*10^{-4}$ A/V^2 and $\mu_p C_{OX} = 3.835*10^{-5}$ A/V^2. 5

c. Derive the gain expression for common drain amplifier.

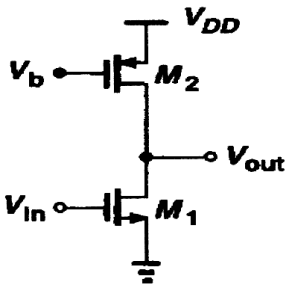

Fig. 1.1

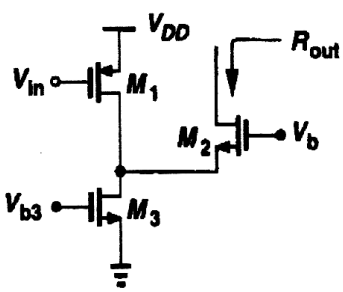

Fig.1.2

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2 a. Draw the small signal model of common gate amplifier with source with source resistance and derive the expression for small signal voltage gain and input resistance of the circuit. Assume $\lambda \neq 0, \gamma \neq 0$. 10

b. Determine the small signal voltage gain of the circuit shown in Fig. 2.1. ($\lambda \neq 0, \gamma \neq 0$). Given $R_F = 5$ kΩ , $R_D = 10$ kΩ, $r_{O1} = 20$ kΩ, and gm = 5 mA/V. 5

c. Derive an expression for the voltage gain of the circuit shown in Fig. 2.2. Assume the following device parameter $(W/L)_{1,2,3} = 30$, $\lambda \neq 0$, $\gamma = 0$ and $I_D = 1$ mA. $\mu_n C_{OX} = 100$ μA/V^2 and $\lambda_n = 0.01$V^{-1}.

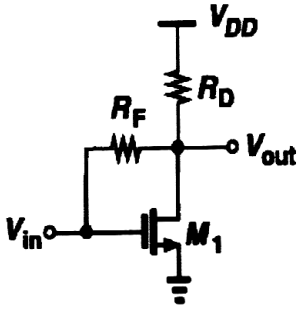

Fig. 2.1

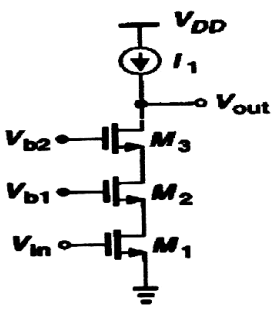

Fig.2.2

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UNIT - II

3 a. For the differential amplifier circuit with resistive loads, derive an expression for $I_{D1}-I_{D2}$ in terms of $V_{G1}-V_{G2}$. Calculate the short circuit transcendence for $V_{G1}-V_{G2}=0$. 12

b. In the circuit shown in Fig. 3.1, assume $I_{SS}=1$ mA and W/L = 50/0.5 for all of the transistors.

i) Determine the circuit voltage gain. Assume $\mu nC_{0x}=350\ \mu A/V^2$, $\mu_P C_{ox}=100\ \mu A/V^2$

ii) Calculate V_b such $I_{D5}=I_{D6}=0.8(I_{ss}/2)$. $\mu_p C_{0x}=38.3\mu A/V^2$ and $V_{THP}=0.8V$ 5

iii) If I_{ss} requires a minimum voltage of 0.4 V, what is the maximum differential output swing?

c. Calculate the small signal voltage gain of the circuit shown in Fig. 3.2

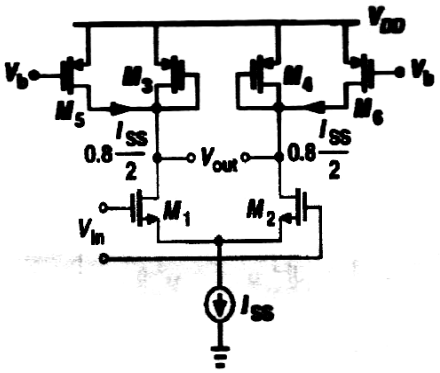

Fig.3.1

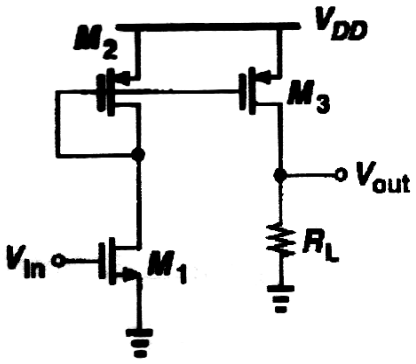

Fig.3.2

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4 a. Illustrate the significance of active and passive current mirrors in amplifier with a suitable example. 15

b. Calculate the differential voltage gain A_v for the circuit shown in Fig. 4.1. Given $I_{ss}=1$ mA, $(W/L)_{1,2}=50/0.5$, $(W/L)_{3,4}=50/1$. Assume $\lambda_N=\lambda_P=0.01\ V^{-1}$, $\mu C_{OX}=100\ \mu A/V^2$, $\mu_P Cox=50\ \mu A/V^2$.

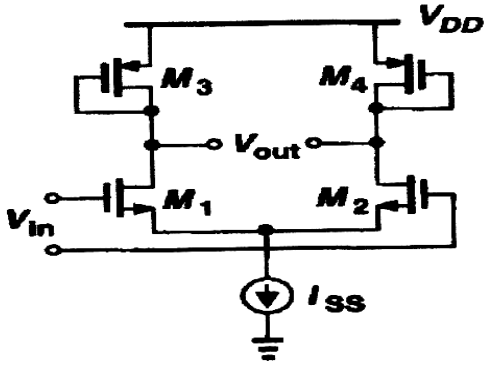

Fig.4.1

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UNIT - III

5 a. Design a fully differential telescopic op-amp with the following specifications:

$V_{DD}=3$ V, Maximum differential swing = 3, total power dissipations = 10 mW. Assume $\mu_n C_{OX}=30\ \mu A/V^2$, $\lambda_N=0.1\ V^{-1}$, $\lambda_P=0.2\ V^{-1}$, $\gamma=0$, $V_{THN}=|V_{THP}|=0.7$ V and $\gamma=0$. Calculate the voltage gain and the required bias voltage V_{b1} and V_{b2}. Note $V_{ov3}=V_{ov1}=0.2$ V, $V_{ov9}=0.5$ V, $|V_{ov7}|=|V_{ov5}|=0.3$. 10

Contd…3

b. Determine the small signal voltage gain of the two stage op-amp shown in Fig. 5.1. Assume $\gamma = 0$, $(W/L)_{1,2} = 50/0.6$, $(W/L)_{3,4} = 10/0.6$, $(W/L)_{5,6} = 20/0.6$ and $(W/L)_{7,8} = 56/0.6$, $\mu_N Cox = 75\ \mu A/V^2$, $\mu_P Cox = 30\ \mu A/V^2$ and $|V_{THP}| = 0.7$ V. 5

c. Calculate the voltage gain A_V for the circuit shown in Fig. 5.2. Given $(W/L)_{1,2,3} = 100/0.5$, $(W/L)_P = 50/0.5$, $\mu_P Cox = 60\mu A/V^2$, $\mu_P Cox = 30\mu A/V^2$, $\lambda_N = 0.1\ V^{-1}$ and $\lambda_P = 0.2V^{-1}$. 5

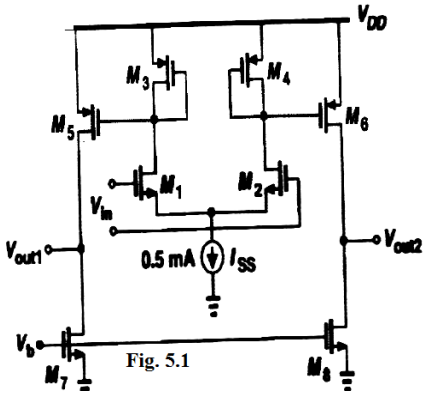

Fig. 5.1

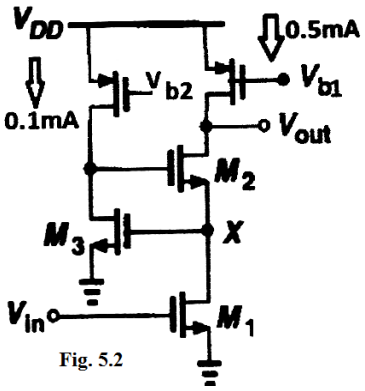

Fig. 5.2

6 a. Identify the type of amplifier in Fig. 6.1, employed in boosting the gain. Also calculate the output impedance at the drain of transistor M3 (Replace ideal current sources with transistors for the calculation) Assume $gm_N = 1$ mA/V, $gm_P = 2$ mA/V and $r_{ON} = 5\ k\Omega$, $r_{OP} = 10\ k\Omega$ 5

b. Calculate the low frequency PSRR of the feedback circuit shown in Fig. 6.2, Assume $C_1 = 10$ pF, $C_2 = 40$ pF, $gm_2 = 1$ mA/V and $r_{o4} = 10\ k\Omega$.

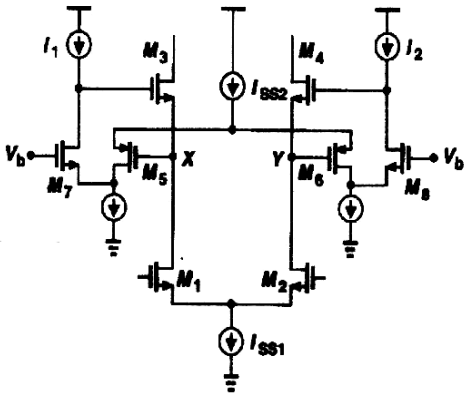

Fig.6.1

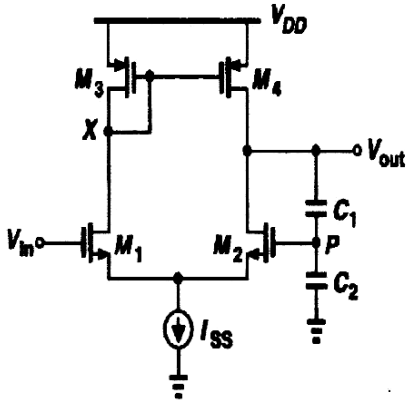

Fig.6.2

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c. Explain the need of common mode feedback in amplifiers. Shown a conceptual topology for the same. 5

UNIT - IV

7 a. With a neat sketch, explain three stage ring oscillator. 10

b. Define voltage controlled oscillator and explain the important performance parameters of VCO's. 10

8 a. Draw the small signal model of Colpitts oscillator and derive an expression for the V_{out}/ I_{in}, $\omega^2 R$ and $g_m R_P$. 10

b. A VCO senses a small sinusoidal control voltage $V_{cont} = V_m \cos \omega_m t$. Determine the output waveform and its spectrum. 10

Contd…4

UNIT - V

9 a. Consider the PLL in the Fig. 9.1 where K_{PD} = 0.5 V/rad, R = 100 Ω and C =100 nF for the filter and K_{VCO} = 10 Mrad/s/V.

i) What is the type and order of this PLL

ii) What is the approximate bandwidth of the PLL

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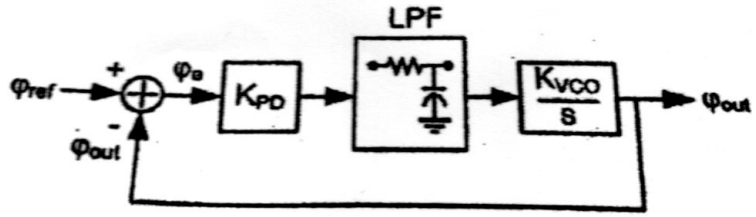

Fig.9.1

b. A cellular telephone incorporates a 900 MHz phase-locked loop to generate the carrier frequencies. If $\omega_{LPF} = 2\pi$ x (20 kHz) and the output frequency is to be changed from 901 MHz to 901.2 MHz, how long does the PLL output frequency take to settle within 100 Hz its final value.? 4

c. Draw and explain the linear model of simple charge pump PLL and obtain the open loop transfer function and closed loop transfer function. 10

10 a. What is PLL? Explain basic PLL topology. 10

b. Explain the skew and jitter reduction of locked loop system. 10

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