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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Seventh Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; Dec. - 2019

Low Power VLSI Design

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a. Explain the need for low power VLSI Design. 5

b. With neat diagram, explain the structure of MIS diode. Draw the energy band diagram of biased MIS Diode. 10

c. Derive an equation for the depth of the depletion region. 5

2 a. Explain the concept of body effect in long channel MOSFET. 4

b. Derive an expression for short circuit and dynamic power dissipation of a CMOS. 8

c. Discuss the overall Load Capacitance of the inverter. 8

UNIT - II

3 a. Explain the conceptual level diagram of possible improvement in power dissipation at various levels. 6

b. Explain with it data flow graph of transposed direct from FIR computation. 8

c. Derive the first order difference algorithm for a discrete LTI-FIR system. 6

4 a. Explain the power optimization using driven voltage scaling. 10

b. Explain the power optimization using operation reduction and operation substitution. 10

UNIT - III

5 a. Analyze the power consumption of CMOS gates for the function $Y = \overline{(X_1 + X_2)X_3}$. 8

b. Explain the following terms in transistor reordering:

i) Delay

ii) Optimization algorithm

iii) Power consumption 6

c. Explain how transistor sizing plays an important role in power dissipation minimization? 6

6 a. Explain the ratio-logic using only NMOS and pseudo NMOS logic network. 6

b. Explain with neat diagram and silent features of the Domino logic and differential current switch logic. 8

c. What are the factor influencing leakages current in deep sub micrometer transistor? 6

Contd…2

UNIT - IV

7	a.	Explain the low voltage design techniques with respect to reverse V_{gs}, Steeper sub-threshold swing in MOS circuits.	10
	b.	Write a note on multiple supply voltages.	10
8	a.	Explain organization of a static RAM.	8
	b.	Draw the circuit diagram of 6 T-SRAM cells.	4
	c.	Discuss the banking organization of SRAM.	8

UNIT - V

9	a.	Discuss how the energy dissipation in transistor channels using an RC model?	6
	b.	Design NAND gate using adiabatic switching for reversible logic.	6
	c.	Explain the generic resonant scheme for adiabatic clock generation circuit.	8
10	a.	Explain various factors essential for software power estimation.	10
	b.	Explain any two software power optimization with suitable example.	10

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