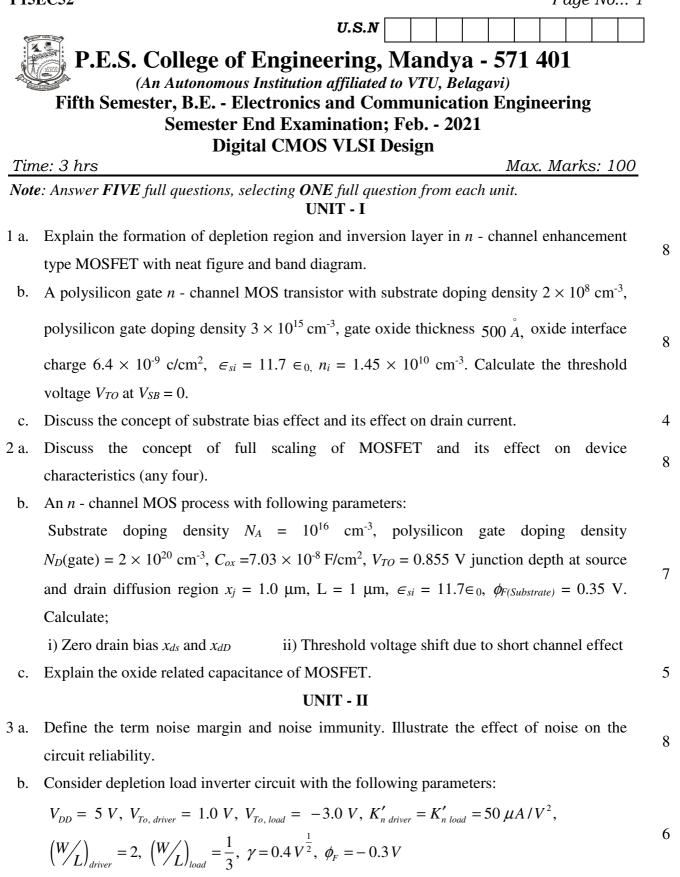
Calculate;

i) Voh



c. Draw the circuit of CMOS inverter and explain its operation with voltage transfer characteristics.

ii) V<sub>OL</sub>

4 a. Discuss the calculation of propagation delay time for high to low output transition  $\tau_{PHL}$  along related waveforms and equations.

Contd...2

6

8

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b.	Explain the calculation of interconnect delay using Elmore delay method.	8
c.	Write the importance of power delay product PDP in CMOS process.	4
	UNIT - III	
5 a.	Write the CMOS NOR2 gate and its inverter equivalent. Obtain the equation for its switching threshold voltage.	6
b.	Design the CMOS circuit for the following:	
	i) $F = \overline{(C+D)E + AB}$ ii) $Z = A \oplus B$	6
c.	Explain the operation of CMOS transmission gate for different bias conditions and operating regions.	8
6 a.	Discuss the small signal analysis of two inverter bistable circuit along with related equation and diagrams.	8
b.	Write the circuit of CMOS negative (falling) edge triggered master slave D flip flop and explain its working.	8
c.	Write the Gate-level schematic and AOI based implementation of the clocked NOR-based SR latch circuit.	4
	UNIT - IV	
7 a.	Analyze the pass transistor circuit for logic '0' transfer and calculate the fall time.	8
b.	Explain the voltage bootstrapping with relevant equations.	8
c.	Write note on charge leakage from the soft node.	4
8 a.	Explain the operation of rationed and ratioless synchronous dynamic logic along with circuit diagram.	8
b.	Discuss the working of NP-Domino logic.	6
c.	Explain the general circuit structure and clock signals of zipper CMOS circuits.	6
	UNIT - V	
9 a.	Explain the working of conventional BiCMOS inverter circuit with active base pull-down.	7
b.	Write the circuit diagram for the following:	
	i) BiCMOS NOR2 gate	6
	ii) BiCMOS NAND2 gate	
c.	Analyze the BJT operating in saturation mode using Ebers-Moll equivalent circuit diagram.	7
10 a.	Discuss the different models for ESD testing.	8
b.	Explain the output circuit and $L(\frac{di}{dt})$ noise.	8
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