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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Fifth Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; Feb. - 2021

Digital CMOS VLSI Design

Time: 3 hrs *Max. Marks: 100*

***Note**: Answer **FIVE** full questions, selecting **ONE** full question from each unit.*

UNIT - I

1 a. Explain the formation of depletion region and inversion layer in *n* - channel enhancement type MOSFET with neat figure and band diagram. 8

b. A polysilicon gate *n* - channel MOS transistor with substrate doping density 2×10^8 cm^{-3}, polysilicon gate doping density 3×10^{15} cm^{-3}, gate oxide thickness $500\ \mathring{A}$, oxide interface charge 6.4×10^{-9} c/cm^2, $\epsilon_{si} = 11.7\ \epsilon_0$, $n_i = 1.45 \times 10^{10}$ cm^{-3}. Calculate the threshold voltage V_{TO} at $V_{SB} = 0$. 8

c. Discuss the concept of substrate bias effect and its effect on drain current. 4

2 a. Discuss the concept of full scaling of MOSFET and its effect on device characteristics (any four). 8

b. An *n* - channel MOS process with following parameters:

Substrate doping density $N_A = 10^{16}$ cm^{-3}, polysilicon gate doping density N_D(gate) $= 2 \times 10^{20}$ cm^{-3}, $C_{ox} = 7.03 \times 10^{-8}$ F/cm^2, $V_{TO} = 0.855$ V junction depth at source and drain diffusion region $x_j = 1.0$ μm, L = 1 μm, $\epsilon_{si} = 11.7\epsilon_0$, $\phi_{F(Substrate)} = 0.35$ V. Calculate; 7

i) Zero drain bias x_{ds} and x_{dD} ii) Threshold voltage shift due to short channel effect

c. Explain the oxide related capacitance of MOSFET. 5

UNIT - II

3 a. Define the term noise margin and noise immunity. Illustrate the effect of noise on the circuit reliability. 8

b. Consider depletion load inverter circuit with the following parameters:

$V_{DD} = 5\ V$, $V_{To,\ driver} = 1.0\ V$, $V_{To,\ load} = -3.0\ V$, $K'_{n\ driver} = K'_{n\ load} = 50\ \mu A/V^2$,

$\left(W/L\right)_{driver} = 2$, $\left(W/L\right)_{load} = \frac{1}{3}$, $\gamma = 0.4\ V^{\frac{1}{2}}$, $\phi_F = -0.3\ V$ 6

Calculate; i) V_{OH} ii) V_{OL}

c. Draw the circuit of CMOS inverter and explain its operation with voltage transfer characteristics. 6

4 a. Discuss the calculation of propagation delay time for high to low output transition τ_{PHL} along related waveforms and equations. 8

Contd…2

b. Explain the calculation of interconnect delay using Elmore delay method. 8

c. Write the importance of power delay product PDP in CMOS process. 4

UNIT - III

5 a. Write the CMOS NOR2 gate and its inverter equivalent. Obtain the equation for its switching threshold voltage. 6

b. Design the CMOS circuit for the following: 6

i) $F = \overline{(C+D)E + AB}$ ii) $Z = A \oplus B$

c. Explain the operation of CMOS transmission gate for different bias conditions and operating regions. 8

6 a. Discuss the small signal analysis of two inverter bistable circuit along with related equation and diagrams. 8

b. Write the circuit of CMOS negative (falling) edge triggered master slave D flip flop and explain its working. 8

c. Write the Gate-level schematic and AOI based implementation of the clocked NOR-based SR latch circuit. 4

UNIT - IV

7 a. Analyze the pass transistor circuit for logic '0' transfer and calculate the fall time. 8

b. Explain the voltage bootstrapping with relevant equations. 8

c. Write note on charge leakage from the soft node. 4

8 a. Explain the operation of rationed and ratioless synchronous dynamic logic along with circuit diagram. 8

b. Discuss the working of NP-Domino logic. 6

c. Explain the general circuit structure and clock signals of zipper CMOS circuits. 6

UNIT - V

9 a. Explain the working of conventional BiCMOS inverter circuit with active base pull-down. 7

b. Write the circuit diagram for the following: 6

i) BiCMOS NOR2 gate

ii) BiCMOS NAND2 gate

c. Analyze the BJT operating in saturation mode using Ebers-Moll equivalent circuit diagram. 7

10 a. Discuss the different models for ESD testing. 8

b. Explain the output circuit and $L\left(di/dt\right)$ noise. 8

c. Write note on H-tree clock distribution technique. 4

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