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P.E.S. College of Engineering, Mandya - 571 401

(An Autonomous Institution affiliated to VTU, Belagavi)

Fifth Semester, B.E. - Electronics and Communication Engineering

Semester End Examination; Feb. - 2021

Digital CMOS VLSI Design

Time: 3 hrs *Max. Marks: 100*

Note: ***I) PART - A*** *is compulsory.* ***Two*** *marks for each question.*

II) PART - B*: Answer any* ***Two*** *sub questions (from a, b, c) for Maximum of* ***18 marks*** *from each unit.*

Q. No.	Questions	Marks
	I : PART - A	**10**
I a.	With the linear and saturation condition for PMOS device, write the drain current expression.	2
b.	Give the critical voltages (V_{IL} and V_{IH}) expression for symmetric CMOS inverter.	2
c.	Implement the 2:1 multiplexer using transmission gates.	2
d.	Design a domino CMOS logic circuit for the Boolean function; $Z = \overline{AB + (C+D)(E+F) + GH}$	2
e.	List out any two causes for latch up problem in CMOS chips.	2
	II : PART - B	**90**
	UNIT - I	**18**
1 a.	Explain the formation of depletion region and inversion layer in an *n*-channel enhancement type MOSFET with neat figure and band diagram.	9
b.	Analyse the oxide related capacitances of MOSFET with relevant equation.	9
c.	Calculate the threshold voltage V_{TO} at V_{SB} = 0, for a polysilicon gate *n*-channel MOS transistor with the following parameters: Substrate doping density $N_A = 10^{16}$ cm^{-3}, Polysilicon gate doping density $N_D = 2 \times 10^{20}$ cm^{-3}, gate oxide thickness $t_{ox} = 500\,\mathring{A}$, and oxide interface fixed charge density $N_{ox} = 4 \times 10^{10}$ cm^{-2}. Assume; $\phi_F(gate) = 0.55\,V, \in_{ox} = 3.97 \in_0, \in_{si} = 11.7 \in_0$ *and* $n_i = 1.45 \times 10^{10}\ cm^{-3}$	9
	UNIT - II	**18**
2 a.	Draw the circuit diagram and VTC indicating critical voltage pointer for CMOS inverter. Analyze the circuit to calculate V_{IL} and V_{IH}.	9
b.	Discuss the calculation of interconnect delay of RC network.	9
c.	For depletion load NMOS inverter with V_{DD} = 5 *V*, $V_{TO,\,driver}$ = 1.0 *V*, $V_{TO,\,load}$ = −3 *V*, $(W/L)_{driver} = 2$, $(W/L)_{load} = 1/3$, $K'_{n\ driver} = K'_{n\ load} = 25\,\mu A/V^2$, $\gamma = 0.4\,V^{1/2}, \phi_F = -0.3\,V, V_{IH} = 2.43\,V$. Calculate the Noise margin.	9

Contd…2

UNIT - III **18**

3 a.	Analyze the CMOS NOR2 gate with relative equation.	9
b.	Analyze the bias conditions and operating regions of CMOS transmission gates.	9
c.	With relevant diagram and equation, explain the behavior of Bistable elements.	9

UNIT - IV **18**

4 a.	Analyze the voltage bootstrapping with relevant equations.	9
b.	Analyze the charge storage and charge leakage phenomenon at a soft node in CMOS network.	9
c.	Analyze the basic principle of operation of NP Domino logic.	9

UNIT - V **18**

5 a.	Discuss the switching delay in BiCMOS logic circuit with related circuit diagram and waveform.	9
b.	Analyze the ESD protection system in CMOS circuit with relevant example.	9
c.	Discuss the process of on-chip clock generation and distribution in CMOS circuit.	9

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